4.5V~65V输入，5A异步降压变换器

65V Input, 5A, Asynchronous Buck Converter

■ FEATURES

- 5A converter with 80mΩ FET
- Input voltage range: 4.5V~65V
- Pulse Skipping Mode (PSM) to keep high efficiency in light load
- 125μA Quiescent Current
- Up to 2MHz Programmable Switching Frequency
- Peak current mode control
- Low Dropout Mode Operation
- Over-voltage , Over-current and Over-Temperature Protection
- Packages: Pb-free Packages, ESOP8

- 5A降压，内置80mΩ功率管
- 输入电压范围：4.5V~65V
- 脉冲跳跃模式使得轻载下高效率
- 125uA静态电流
- 最高2MHz可编程开关频率
- 峰值电流控制架构
- 欠压保护、过流保护和过热关断保护
- 无铅封装，ESOP8

■ APPLICATIONS

- 12V, 24V, 48V Industry and Telecom Power System
- Automotive Systems
- Distributed Power Systems
- High Voltage Power Conversion

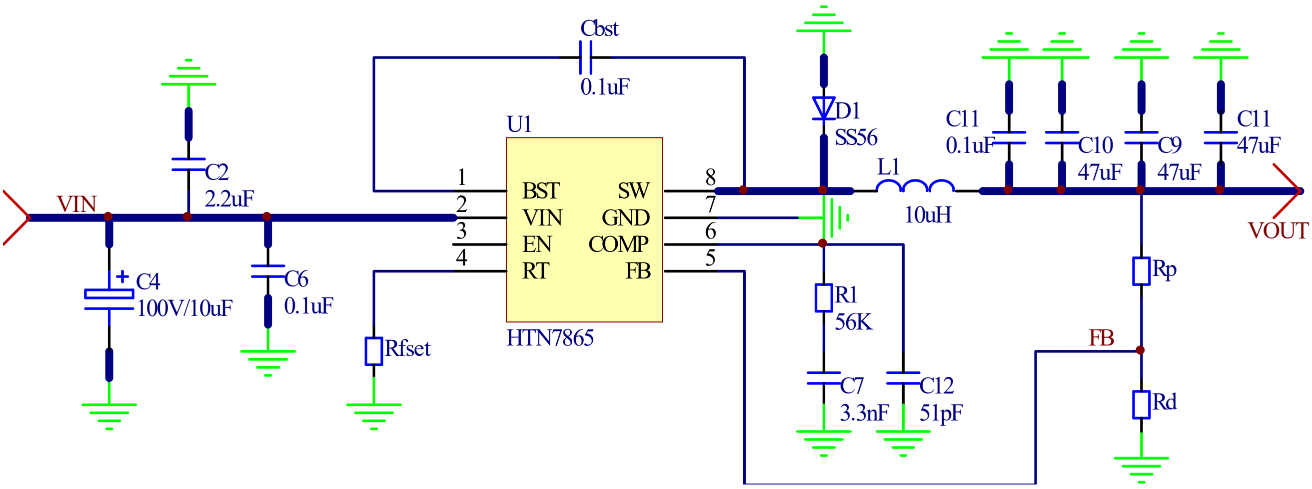
- 12V，24V，48V工业和电信电源轨系统
- 汽车系统
- 分布式电源系统
- 高压电源转换

■ DESCRIPTION

The HTN7865 is 5A buck converters with wide input voltage, ranging from 4.5V to 65V, which integrates an 90mΩ high-side MOSFET. The HTN7865, adopting the peak current mode control, supports the Pulse Skipping Modulation (PSM) which assists the converter on achieving high efficiency at light load. The HTN7865 features programmable switching frequency from 100kHz to 2MHz with an external resistor. The HTN7865 allows power conversion from high input voltage to low output voltage with a minimum 120ns on-time of switch MOS. The device offers typical 2.5ms soft start to prevent inrush current during the startup. The HTN7865 features external loop compensation to provide the flexibility to optimize either loop stability or loop response. The HTN7865 provides cycle-by-cycle current limit, thermal shutdown protection, output over-voltage protection, output over load protection and input voltage under-voltage protection. The device is available in an ESOP8 package.

HTN7865是5A降压转换器，具有从4.5V到65V的宽输入电压，集成了90mΩ高侧MOSFET。HTN7865采用峰值电流模式控制，支持跳周期调制（PSM），有助于转换器在轻负载下实现高效率。HTN7865具有100kHz至2MHz的可编程开关频率，外部电阻可调。HTN7865允许从高输入电压到低输出电压的功率转换，开关MOS的最小导通时间为120ns。该设备提供典型2.5ms的固定软启动，以防止启动过程中的涌入电流。HTN7865具有外部环路补偿功能，可灵活优化环路稳定性或环路响应。HTN7865提供逐周期电流限制、热关断保护、输出过压保护、输出过载保护和输入电压欠压保护。该设备采用ESOP8封装。

■ TYPICAL APPLICATION



1. BST电容C_{BST}典型值0.1uF陶瓷电容
2. VIN输入电容典型值0.1uF//2.2uF陶瓷电容，输入有插拔时建议增加10uF电解电容，并关注VIN端峰值电压不能超过65V
3. EN为芯片使能端

EN	工作状态
悬空、或连接到VIN、或接高	正常工作
接地	关闭

4. RT端设置开关频率，通过R_{FSET}. R_{FSET} = 240k时，F_{SW}≈430kHz

$$FSW(kHz) = \frac{75000}{Rfset(kohm)^{0.94}}$$

5. COMP端设置环路稳定性，一般可直接使用上图典型值，输出不稳定时可使用我司excel工具计算
6. FB端设置升压值

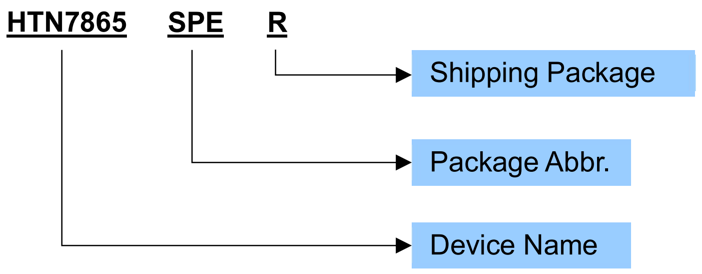
$$VOUT = 0.8 \times \left(1 + \frac{R_P}{R_B}\right)$$

7. 频率设置为400kHz时，电感推荐使用10uH，I_{SAT} > 1.4*I_{OUTmax}
8. 二极管选型：V_{RMS} > 1.2*$_{VINmax}$, I_F > I_{OUTmax}，推荐使用SS56
9. 输出电容推荐使用0.1uF//47uF//47uF//47uF陶瓷电容，建议其额定耐压大于2*VOUT

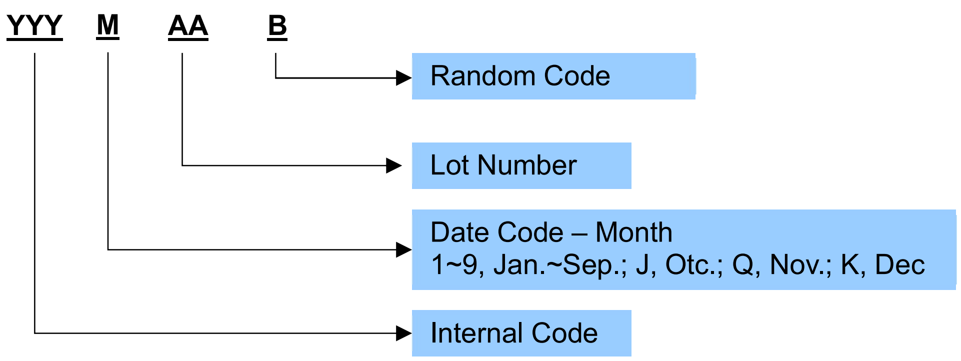
■ ORDERING INFORMATION

Part Number	Package Type	Package Abbr.	Marking	Shipping Package / MOQ
HTN7865SPER	ESOP8	SPE	HTN7865 YYYMAAB[1]	Tape and Reel (R) / 2500pcs

Part Number

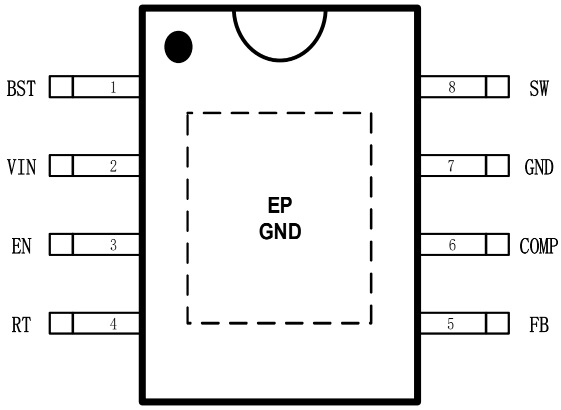


Production Tracking Code



[1] YYYMAAB is production tracking code

■ TERMINAL CONFIGURATION



HTN7865(ESOP8) Top View

■ TERMINAL FUNCTION

Terminal No.	Name	Description
1	BST	Bootstrap. Power supply for the high-side MOSFET driver. Connect a bypass capacitor between BST and SW. BST是内部高端MOSFET驱动器的正电源。在BST和SW之间连接一个旁路电容器。
2	VIN	Input supply. VIN supplies power to all of the internal control circuitries. A decoupling capacitor to ground must be placed close to VIN to minimize switching spikes. 输入电源。VIN为所有内部控制电路供电。接地滤波电容必须放置在VIN附近，以减少开关尖峰。
3	EN	Enable pin to the regulator with internal pull-up current source. Pull below 1.2V to disable the converter. Float or connect to VIN to enable the converter. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold. 稳压器使能引脚，带内部上拉电流源。将电压降至1.2V以下禁用转换器。悬空或连接到VIN可以启动转换器。从VIN到GND的电阻分压抽头连接EN引脚的可以调节输入电压锁定阈值。
4	RT	Set the internal oscillator clock frequency. Connect a resistor from this pin to ground to set switching frequency. 设置内部振荡器时钟频率。将一个电阻从该引脚连接到地，以设置开关频率。
5	FB	Feedback. Connect resistor divider to output voltage. 反馈。接分压电阻到输出电压。
6	COMP	Error amplifier output. Connect to frequency loop compensation network. 误差放大器输出。连接到频率环路补偿网络。
7	GND	Ground. GND should be placed as close to the output capacitor as possible to avoid the high-current switch paths. 地。GND应尽可能靠近输出电容，以避免高电流开关路径。
8	SW	Switch node, connect SW to an external power inductor 开关端口，连接外部功率电感。
EP	GND	Heat dissipation path of die. Electrically connection to GND pin. 芯片散热路径。与GND引脚电气相连。

SPECIFICATIONS[1]

Absolute Maximum Ratings [2]

PARAMETER	Symbol	MIN	TYP	MAX	UNIT
VIN supply voltage	VIN	-0.3		75	V
BST voltage	BST	-0.3		80.5	V
BST voltage (10ns transient)	BST	-0.3		82.5	V
Voltage between BST and SW	BST to SW	-0.3		6	V
FB voltage	FB	-0.3		5.5	V
EN voltage	EN	-0.3		VIN+0.3	V
SW voltage	SW	-2		75	V
SW voltage (10ns transient)	SW	-3.5		77	V
Moisture Sensitivity Level (MSL)			MSL3		
Junction Temperature	T_J	-40		150	℃
Storage Temperature	T_{STG}	-55		150	℃
ESD, Human-body model (HBM)	HBM		±2000		V
ESD, Charged-device model (CDM)	CDM		±500		V

Recommended Operating Conditions

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
VIN supply voltage	VIN		4		65	V
BST voltage	BST		-0.1		70.5	V
Voltage between BST and SW	BST to SW		-0.1		5.5	V
FB voltage	FB		-0.1		4.5	V
EN voltage	EN		-0.1		VIN	V
SW voltage	SW		-1.8		65	V
Junction Temperature	T_J		-40		125	℃

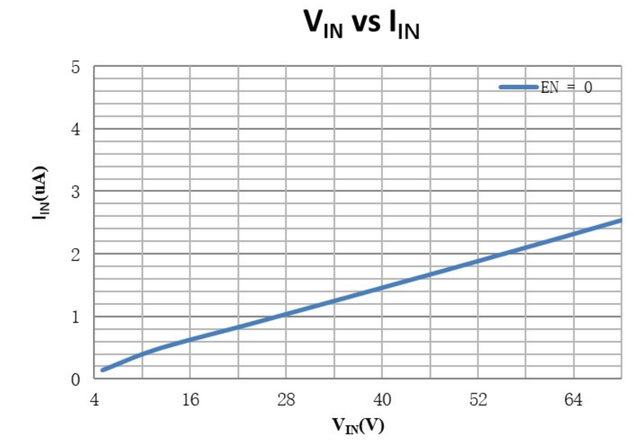
Electrical Characteristics

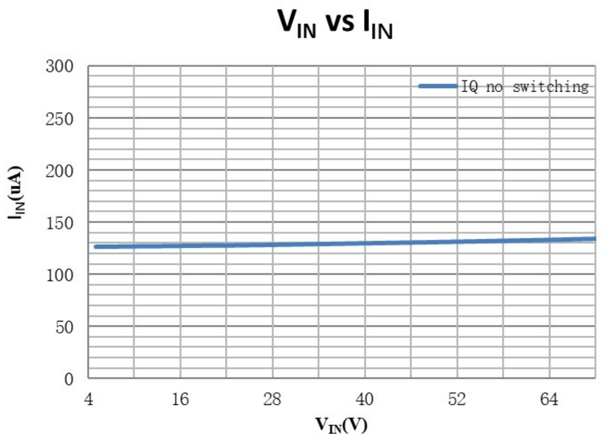
VIN = 12V, T_A = +25°C, unless otherwise noted.

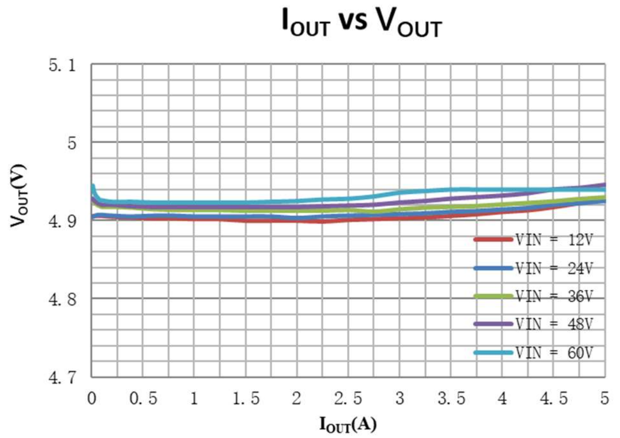
PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
VIN UVLO threshold	V_{UVLO}	Rising		4.5		V
		Falling		4.15		V
VIN UVLO hysteresis	V_{hys}			0.35		V
Quiescent supply current	I_Q	V_{EN} = 12V, V_{FB} = 1.0 V, no switching		125		uA
Shutdown supply current	I_{SD}	V_{EN} = 0V		0.5		μA
High-side switch on resistance	$R_{DS(ON)\_H}$	V_{BST} - V_{SW} = 5.5V		90		mΩ
Peak Current limit	I_{LIM_peak}			7.5		A
EN threshold	V_{ENH}	No voltage hysteresis, rising and falling		1.2		V
EN source current	$I_{source1}$	Enable threshold +50 mV		-4.8		uA
	$I_{source2}$	Enable threshold -50 mV		-1.2		uA
Feedback voltage	V_{FBH}			800		mV
FB input current	I_{FB}	V_{FB} = 0.8V	-100		100	nA
Error Amplifier source/sink		V_{comp} = 1V，Vfb = 0.8±0.1V		±24		uA
Gm of Error Amplifier				210		uS
Minimum on time	t_{ON_MIN}			120		ns
Soft-start time	t_{SS}	Fsw = 500K		2.5		ms
Switching frequency range	f_{sw}		100		2000	kHz
		RT = 200KΩ		500		kHz
Thermal shutdown		Trigger thermal shutdown		165		℃
		Hysteresis		25		℃

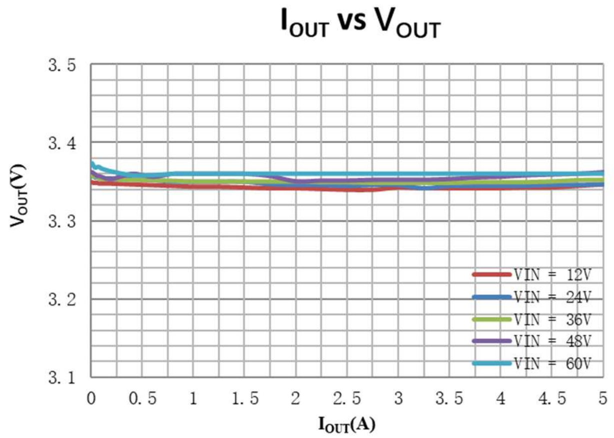
■ TYPICAL OPERATING CHARACTERISTICS

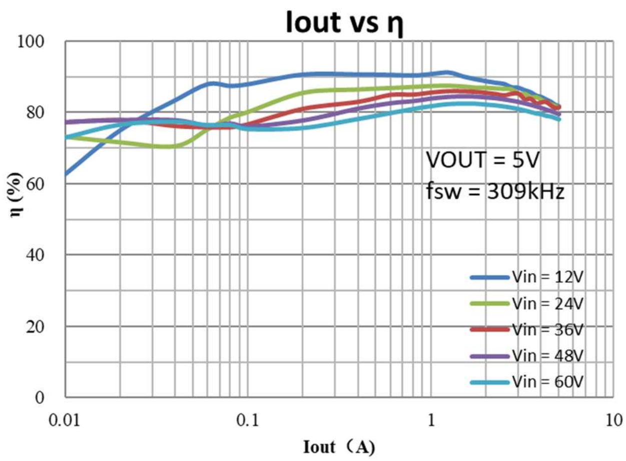
VIN = 12V, VOUT =5V, CIN = 0.1uF//1uF//100μF, COUT = 0.1uF//47uF//47uF, L = 10μH, RT = 240k, Rcomp = 56k, Ccomp = 3.3nF, Cp = 51pF, TA = +25°C, unless otherwise noted.

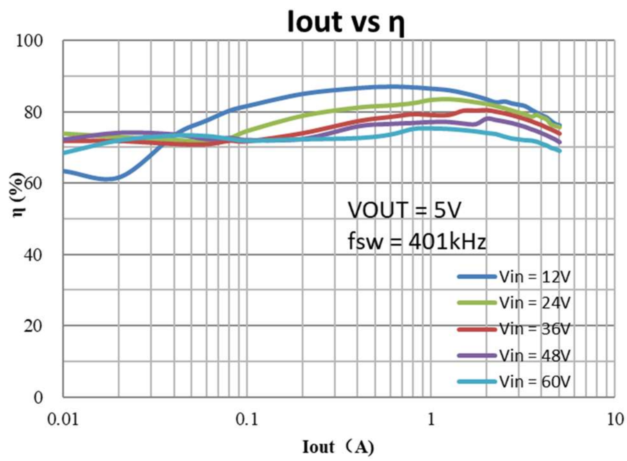












■ APPLICATION INFORMATION

1 Description

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HTN7865 是 5A 降压转换器，具有从 4.5V 到 65V 的宽输入电压，集成了 90mΩ高侧 MOSFET。HTN7865 采用峰值电流模式控制，支持跳周期调制（PSM），有助于转换器在轻负载下实现高效率。HTN7865 具有 100kHz 至 2MHz 的可编程开关频率，外部电阻可调。HTN7865 允许从高输入电压到低输出电压的功率转换，开关 MOS 的最小导通时间为 120ns。该设备提供 2ms 的典型软启动，以防止启动过程中的涌入电流。HTN7865 具有外部环路补偿功能，可灵活优化环路稳定性或环路响应。HTN7865 提供逐周期电流限制、热关断保护、输出过压保护、输出过载保护和输入电压欠压保护。该设备采用 ESOP8 封装。

2 Enable (EN) Control

The HTN7865 is enabled when the VIN pin voltage rises above 4.5V and the EN pin voltage exceeds the enable threshold of 1.2 V. The HTN7865 is disabled when the VIN pin voltage falls below 4.15V or when the EN pin voltage is below 1.2 V. The EN pin has an internal pull-up current source, I1, of 1.2 μA that enables operation of the HTN7865 when the EN pin floats. If an application requires a higher under-voltage lockout (UVLO) threshold, to adjust the input voltage UVLO with two external resistors. When the EN pin voltage exceeds 1.2 V, an additional 3.6μA of hysteresis current, IHYS, is sourced out of the EN pin. When the EN pin is pulled below 1.2 V, the 3.6μA Ihys current is removed. This additional current facilitates adjustable input-voltage UVLO hysteresis.

当 VIN 引脚电压升至 4.5V 以上且 EN 引脚电压超过 1.2 V 的启用阈值时，HTN7865 启用。当 VIN 引脚的电压降至 4.15 V 以下或 EN 引脚的电压低于 1.2 V 时，HTN7865 禁用。EN 引脚有一个 1.2μA 的内部上拉电流源 I1，当 EN 引脚浮空时，它可以使 HTN7865 工作。如果应用需要更高的欠压锁定（UVLO）阈值，则使用两个外部电阻调整输入电压 UVLO。当 EN 引脚电压超过 1.2 V 时，EN 引脚会额外提供 3.6μA 的滞回电流 IHYS。当 EN 引脚被拉到 1.2V 以下时，3.6μA 的电流被移除。这种额外的电流有助于调节输入电压 UVLO 滞回。

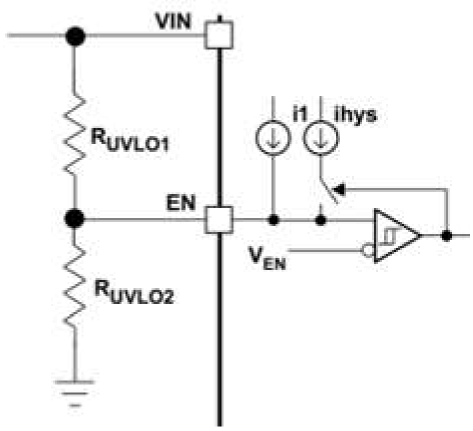


Figure 1 EN Terminal Schematic

3 Soft Start and Start Delay with Pre-biased Output Voltage

The HTN7865 employs an internal soft start to ramp up the FB voltage from 0V to 0.8V linearly once EN pulled high.

If the output voltage is pre-biased when EN is pulled high, the device start switching and ramping up only after internal reference voltage is larger than V_{FB}.

HTN7865 采用内部软启动，一旦 EN 拉高，FB 电压就会线性上升至 0.8V。

如果 EN 被拉高时输出有预偏置电压，器件仅在内部基准电压大于 V_{FB} 后开始工作。

4 Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at an insufficient supply voltage. The UVLO rising threshold is about 4.5V, while its falling threshold is about 4.15V.

欠压锁定（UVLO）功能可避免芯片工作在电源电压不足的条件。UVLO 上升阈值约为4.5V，下降阈值为 4.15V。

5 Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than its upper threshold, the entire chip shuts down. When the temperature is lower than its lower threshold, the chip is enabled again.

过热关断保护是为了防止芯片在极高的温度下工作。当芯片温度高于其上限阈值时，整个芯片关闭。当温度低于其下限阈值时，芯片再次启用。

6 Peak Current Mode Control

The HTN7865 employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the integrated high-side MOSFET is turned off. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent subharmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control. The HTN7865 operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. When the load current decreases, an increment in the feedback voltage leads COMP voltage drop. When COMP falls to a low clamp threshold (700mV typically), device enters PSM. The output voltage decays due to output capacitor discharging during skipping period. Once FB voltage drops lower than the reference voltage, and the COMP voltage rises above low clamp threshold. Then high-side power MOSFET turns on in next clock pulse. After several switching cycles, COMP voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded. This control scheme helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. The controller consumption quiescent current is 125uA during skipping period with no switching to improve efficiency further.

HTN7865 采用固定频率峰值电流模式控制。内部时钟在每个周期启动内部高侧功率 MOSFET 的开启，然后电感器电流线性上升。当通过高侧 MOSFET 的电流达到由内部误差放大器的 COMP 电压设置的阈值水平时，集成的高侧 MOSFET 被关断。当负载电流增加时，相对于参考电压的反馈电压降低会提高 COMP 电压，直到平均电感器电流与增加的负载电流相匹配。该反馈回路很好地将输出电压调节到参考值。该设备还集成了一个内部斜坡补偿电路，以防止在固定频率峰值电流模式控制的占空比大于 50%时发生次谐波振荡。HTN7865 在轻负载电流下以脉冲跳过模式（PSM）运行，以提高效率。当负载电流降低时，反馈电压的增加导致 COMP 电压降。当 COMP 降至低箝位阈值（通常为 700mV）时，设备进入 PSM。在跳跃期间，由于输出电容器放电，输出电压衰减。一旦 FB 电压降至低于参考电压，并且 COMP 电压升至低箝位阈值以上，高侧功率 MOSFET 在下一个时钟脉冲中导通。在几个开关周期后，COMP 电压下降并再次被箝位，如果输出继续轻载，则重复跳周期模式。这种控制方案通过跳过周期来减少开关功率损耗和栅极驱动充电损耗，从而有助于实现更高的效率。控制器在跳过期间消耗的静态电流为 125uA，无需切换，以进一步提高效率。

7 Bootstrap Voltage Regulator and Low Drop-out Operation

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and the external low-side diode conducts. The recommended value of the BOOT capacitor is 0.1μF. The UVLO of high-side MOSFET gate driver has rising threshold of 2.6V and hysteresis of 210mV. When the device operates with high duty cycle or extremely light load, bootstrap capacitor may be not recharged in considerable long time. The voltage at bootstrap capacitor is insufficient to drive high-side MOSFET fully on. When the voltage across bootstrap capacitor drops below 2.39V, BOOT UVLO occurs. The converter forces turning on an integrated low-side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee the converter's operation over a wide duty range. During the condition of ultra-low voltage difference from the input to the output, HTN7865 operates in Low Drop-Out LDO mode. High-side MOSFET remains turning on as long as the BOOT pin to SW pin voltage is higher than BOOT UVLO threshold 2.6V. When the voltage from BOOT to SW drops below 2.39V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor periodically in the following several switching cycles. Low-side MOSFET only turns on for 200ns in each refresh cycle to minimize the output voltage ripple. Low-side MOSFET may turn on for several times till the bootstrap voltage is charged to higher than 2.6V for high-side MOSFET working normally. The effective duty cycle of the converter during LDO operation can be approaching to 100%. During slowing power up and power down application, the output voltage can closely track the input voltage ramping down thanks to LDO operation mode.

BOOT 引脚和 SW 引脚之间的外部自举电容器为高侧功率 MOSFET 的浮栅驱动器供电。当高侧功率 MOSFET 关断并且外部低侧二极管导通时，自举电容器电压从集成电压调节器充电。BOOT 电容器的推荐值为 0.1μF。高侧 MOSFET 栅极驱动器的 UVLO 具有 2.6V 的上升阈值和 210mV 的滞后。当设备以高占空比或极轻负载运行时，自举电容器可能在相当长的时间内无法再充电。自举电容器上的电压不足以驱动高压侧 MOSFET 完全导通。当自举电容上的电压降至 2.39V 以下时，会发生 BOOT UVLO。转换器周期性地强制开启集成低压侧 MOSFET，以刷新自举电容器的电压，从而保证转换器在宽占空比范围内的运行。在输入到输出的超低电压差条件下，HTN7865 以低压差 LDO 模式运行。只要 BOOT 引脚到 SW 引脚的电压高于 BOOT UVLO 阈值 2.6V，高侧 MOSFET 就会保持导通。当从 BOOT 到 SW 的电压降至 2.39V 以下时，高压侧 MOSFET 关断，低压侧 MOSFET 接通，在接下来的几个开关周期内定期对自举电容器进行充电。低侧 MOSFET 在每个刷新周期中仅导通 200ns，以尽量减少输出电压纹波。低侧 MOSFET 可能会导通几次，直到自举电压充电到高于 2.6V，以便高侧 MOSFET 正常工作。LDO 操作期间转换器的有效占空比可以接近 100%。在缓慢加电和断电应用期间，由于 LDO 操作模式，输出电压可以密切跟踪输入电压的下降。

8 Over Current and Short Protection

To protect the converter in overload conditions at higher switching frequencies and input voltages, the HTN7865 implements a frequency fold-back. The oscillator frequency is divided by 1, 2, 4, and 8 as the FB pin voltage falls from 0.8 V to 0 V. The HTN7865 uses a digital frequency fold-back to enable synchronization to an external clock during normal start-up and fault conditions. During short-circuit events, the inductor current can exceed the peak current limit because of the high input voltage and the minimum controllable on-time. When the output voltage is forced low by the shorted load, the inductor current decreases slowly during the switch off-time. The frequency fold-back effectively increases the off-time by increasing the period of the switching cycle providing more time for the inductor current to ramp down.

为了在较高开关频率和输入电压下的过载条件下保护转换器，HTN7865 实现了频率折返。当 FB 引脚电压从 0.8 V 降至 0 V 时，振荡器频率会分频，有 1、2、4 和 8 四种。HTN7865 使用数字频率折返，在正常启动和故障条件下与外部时钟同步。在短路事件期间，由于高输入电压和最小可控导通时间，电感器电流可能超过峰值电流限制。当短路负载迫使输出电压降低时，电感器电流在关断时间内缓慢下降。频率回折通过增加开关周期的周期有效地增加了关断时间，为电感器电流斜坡下降提供了更多时间。

9 Clock Setting

The HTN7865 oscillating frequency is set by an external resistor R_{fset}, from the RT pin to ground. The value of R_{fset} can be set according to the following equation or curve.

HTN7865 的开关频率可通过 RT 对地电阻 Rfset 调节，参考如下公式或曲线图。

$$FSW(kHz) = \frac{75000}{Rfset(kohm)^{0.94}} \quad (1)$$

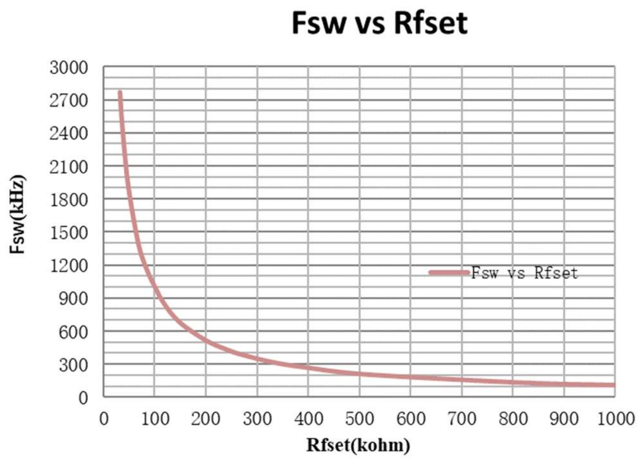


Figure 2 Fsw vs Rfset

10 Setting the Output Voltage

The output voltage (V_{OUT}) is set by a resistor divider (R_P and R_B). The resistors can be determined with following Equation.

Where V_{FB} is 0.8V, typically.

输出电压 （VOUT） 由电阻分压器（R_P 和 R_B）设置。 电阻可以通过以下公式确定。

其中，V_{FB} =0.8V。

$$VOUT = V_{FB} \times \left(1 + \frac{R_P}{R_B}\right) \quad (2)$$

11 Selecting the Inductor, Diode and Output Capacitor

Use the inductor and output capacitor as following.

推荐电感和输出电容如下表。

OUTPUT VOLTAGE (V)	R_P (kΩ)	R_B(kΩ)	L (uH)			C_{OUT}(uF)
			MIN	TYP	MAX	
1.8	66.5	53.6	6.8	10	15	⩾44
2.5	61.9	29.4	6.8	10	15	⩾44
3.3	127	40.2	6.8	10	15	⩾44
5	48.7	9.31	6.8	10	15	⩾66
12	140	10	10	15	22	⩾100

The HTN7865 requires an external rectifier diode between SW and GND. The reverse voltage of the diode should be greater than the maximum input voltage, and the current rating should be higher than the maximum load current.

HTN7865 需要外部整流二极管，放置在 SW 和 GND 之前。二极管的反向电压需大于最大输入电压，额定电流英大于最大负载电流。

The inductor peak-to-peak ripple current I_{L_PP}, peak current I_{L_PK} and RMS current I_{L_RMS} are calculated as following. The inductor saturation current rating must be greater than the I_{L_PK} and the RMS or heating current rating must be greater than I_{L_RMS}.

电感峰峰值电流 I_{L_PP}、峰值电流 I_{L_PK} 和 RMS 电流 I_{L_RMS} 计算如下。电感额定饱和电流必须大于 I_{L_PK}，RMS 或热电流额定值必须大于 I_{L_RMS}。

$$I_{L_{PP}} = \frac{V_{OUT}}{V_{IN_{MAX}}} \times \frac{V_{IN_{MAX}} - V_{OUT}}{L \times f_{SW}} \quad (3)$$

$$I_{L_{PK}} = I_{OUT} + \frac{I_{L_{PP}}}{2} \quad (4)$$

$$I_{L_{RMS}} = \sqrt{I_{OUT}{}^2 + \frac{1}{12} \times I_{L_{PP}}{}^2} \quad (5)$$

The output capacitor should be used with ceramic or other low ESR capacitors. The required RMS current rating for the output capacitor is as follow.

输出电容应使用陶瓷电容或其他低 ESR 电容。输出电容要求的额定 RMS 电流如下。

$$I_{C_{RMS}} = \frac{\left(V_{IN_{MAX}} - V_{OUT}\right) \times V_{OUT}}{\sqrt{12} \times F_{SW} \times V_{IN_{MAX}} \times L} \quad (6)$$

12 Input Capacitor (C_{IN})

An input decoupling capacitor (0.1uF) and a bulk capacitor (Over 10uF) is needed. The voltage rating should be higher than the maximum input voltage.

输入端推荐一个滤波电容（0.1uF）和一个储能电容（超过 10uF）。额定电压应高于最大输入电压。

13 PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to following figure and follow the guidelines below.

(1) Place the input capacitor and output capacitor as close to the device as possible.

(2) Keep the power traces very short and fairly wide, especially for the SW node.

This can help greatly reduce voltage spikes on the SW node and lower the EMI noise level.

(3) Run the feedback trace as far from the inductor and noisy power traces (like the SW node) as possible.

有效的 PCB 布局对于稳定运行至关重要。要获得最佳结果，请参考下图并遵循以下指南。

（1）将输入电容、输出电容尽可能靠近芯片。

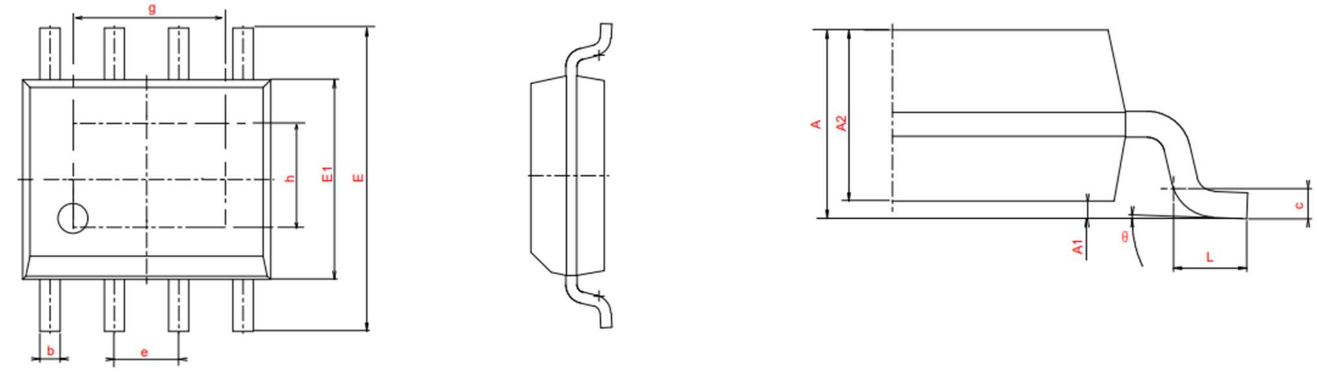
（2）保持电源轨迹非常短且相当宽，特别是对于 SW 节点。

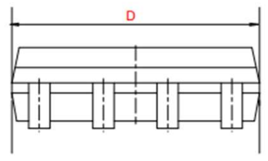
这有助于大大降低 SW 节点上的电压尖峰，并降低 EMI 噪声水平。

（3）FB 走线尽可能远离电感和功率走线（如 SW 节点）。

■ PACKAGE OUTLINE

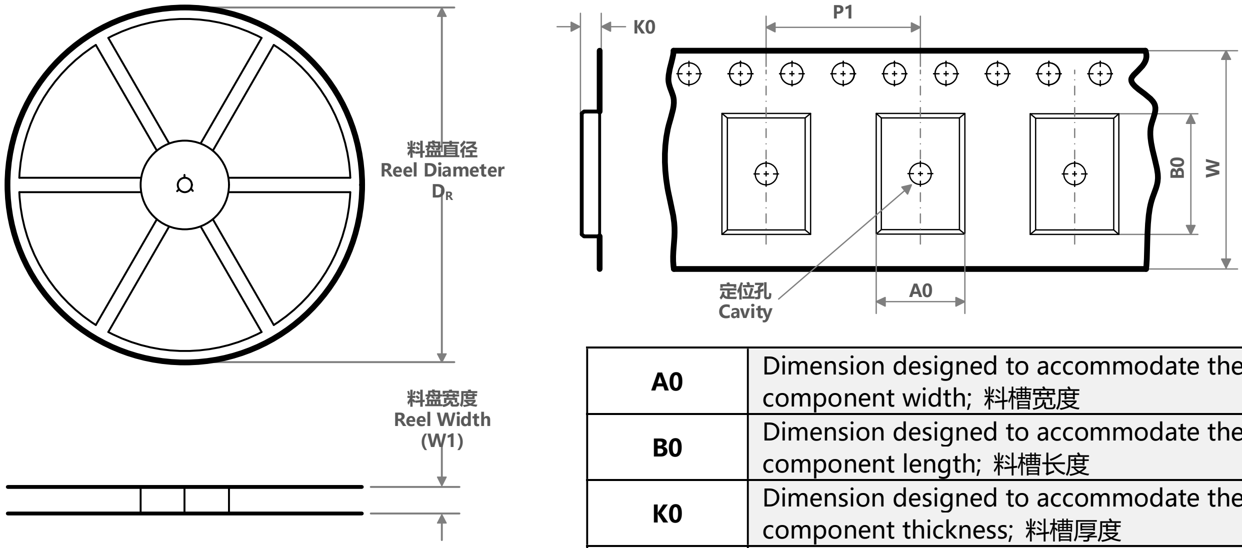
ESOP8





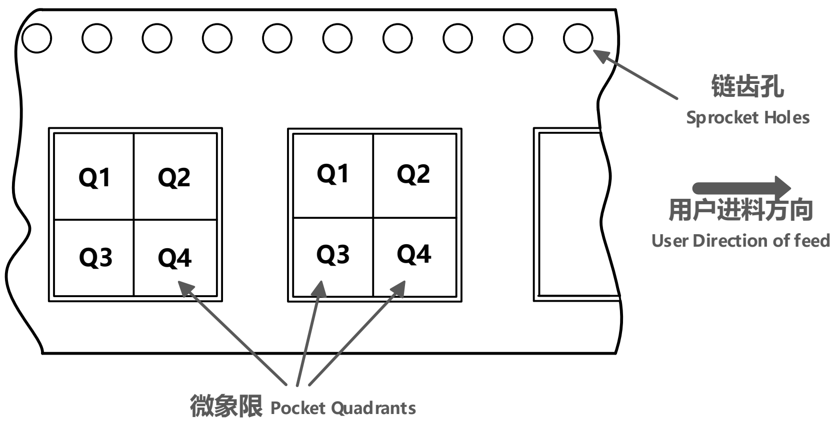
名称	尺寸	
	Min	Max
A	1.45	1.75
A1	0.05	0.15
A2	1.35	1.55
b	0.3	0.5
c	0.22	0.28
D	4.7	5.1
E	5.8	6.2
E1	3.85	4.05
L	0.4	1.27
θ	0°	8°
e	1.270 (BSC)	
h	2.4	
g	3.3	

■ TAPE AND REEL INFORMATION



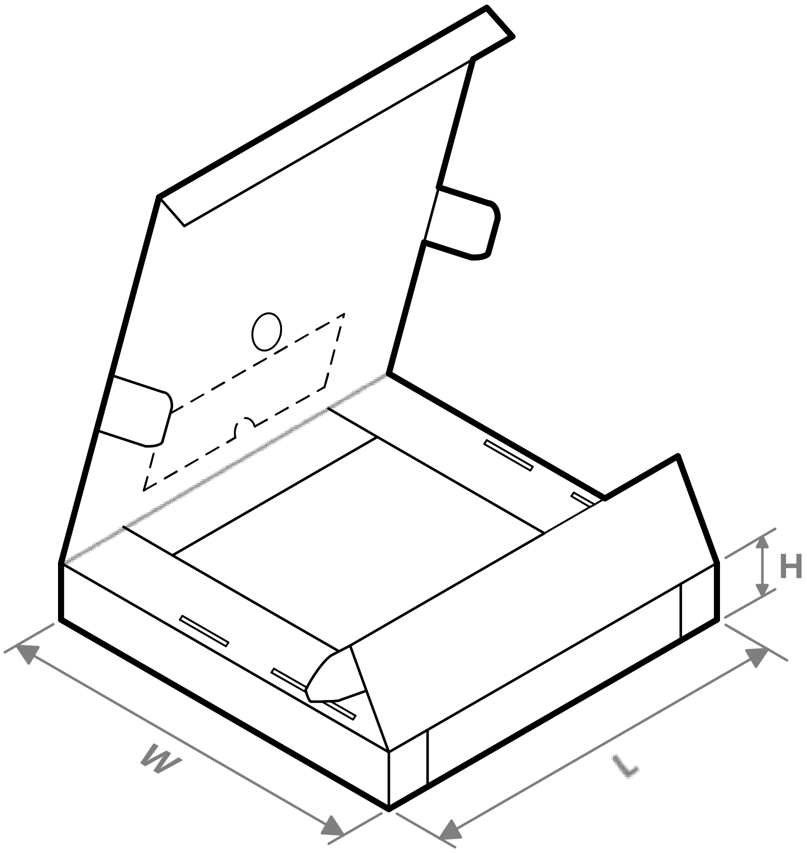
A0	Dimension designed to accommodate the component width; 料槽宽度
B0	Dimension designed to accommodate the component length; 料槽长度
K0	Dimension designed to accommodate the component thickness; 料槽厚度
W	Overall width of the carrier tape; 载带整体宽度
P1	Pitch between successive cavity centers; 相邻槽中心间距

编带 PIN1 方位象限分配
Quadrant Assignments for Pin1 Orientation in Tape



器件料号 Part No.	封装类型 Package Type	封装标识 Package Code	引脚数 Pins	SPQ	料盘直径 DR(mm)	料盘宽度 W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 象限 Quadrant
HTN7865SPER	ESOP	SPE	8	2500	330	12	6.55	5.55	1.95	8	12	Q1

■ TAPE AND REEL BOX INFORMATION



器件料号 Part No.	封装类型 Package Type	封装标识 Package Code	引脚数 Pins	SPQ	长度 Length (mm)	宽度 Width (mm)	高度 Height (mm)
HTN7865SPER	ESOP	SPE	8	5000	360	345	65

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