带输出关断的20V, 14A全集成同步升压转换器

■ 特点

- 输入电压范围V_{PIN}：2.7V-20V
- 输出电压范围V_{OUT}：4.5V-20V
- 可编程峰值电流：14A
- 高转换效率：
  95% (V_{PIN} = 7.2V, V_{OUT}=16V, I_{OUT} =3A)
  94% (V_{PIN} = 12V, V_{OUT}=18V, I_{OUT} =4A)
  90% (V_{PIN} = 3.3, V_{OUT}=9V, I_{OUT} =3A)
- 轻载条件下两种调制方式：脉频调制（PFM）和强制脉宽调试（PWM）
- 集成输出关断的栅极驱动
- 低关断功耗，关断电流1uA
- 可调节的开关频率：200k-1.4M
- 可编程软启动
- 输出过压 (22V)、逐周期过流、热关断等保护
- QFN3.5×4.5-20L，无铅超薄封装

■ 应用

- 无线音箱
- 便携式音箱
- 快充移动电源
- 电子烟
- USB TYPE-C 电源传输
- 拉杆音箱
- 平板电脑，笔记本电脑
- POS机终端

■ 概述

HT7178是一款高功率、全集成升压转换器，带有负载关断功能的栅极驱动，集成16mΩ功率开关管和16mΩ同步整流管，为便携式系统提供高效的小尺寸解决方案。

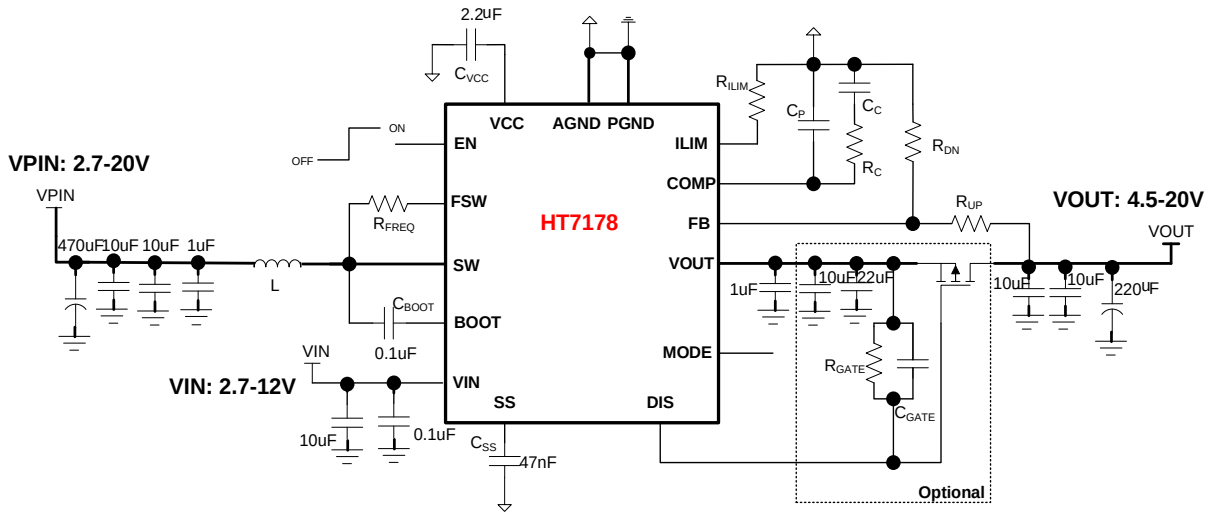
HT7178具有2.7V至20V宽输入电压范围，可为采用单节或两节锂电池，或12V铅酸电池的应用提供支持。该器件具备14A开关电流能力，并且能够提供高达20V的输出电压。

HT7178采用自适应恒定关断时间峰值电流控制拓扑结构来调节输出电压。在中等到重负载条件下，HT7178 工作在PWM 模式。在轻负载条件下，该器件可通过MODE引脚选择下列两种工作模式之一。一种是可提高效率的PFM模式；另一种是可避免因开关频率较低而引发应用问题的强制PWM模式。PWM模式下，HT7178的开关频率可通过外部电阻调节，支持200kHz至1.4MHz的范围。

HT7178还支持可编程的软启动，以及可调节的开关峰值电流限制。另外，HT7178集成了输出关断功能的栅极驱动，在SD状态，可完全断开输入电源。

此外，该器件还提供有22V输出过压保护、逐周期过流保护和热关断保护。

■ 典型应用图



20V,14A Fully-Integrated Synchronous Boost Converter with Load Disconnect Control

FEATURES

- Input voltage range V_{PIN}: 2.7V to 20V
- Output voltage range V_{OUT}: 4.5V to 20V
- Programmable switch peak current limit: up to 14A
- High Efficiency
  - 95% (V_{PIN} = 7.2V, V_{OUT}=16V, I_{OUT} =3A)
  - 94% (V_{PIN} = 12V, V_{OUT}=18V, I_{OUT} =4A)
  - 90% (V_{PIN} = 3.3, V_{OUT}=9V, I_{OUT} =3A)
- 2 modulation mode available: PFM or PWM mode at light load
- Integrated gate driver for load disconnect and output short protection
- 1.0μA current consumption during shutdown
- Adjustable switching frequency: 200k to 1.4MHz
- Programmable soft start
- Output overvoltage protection (at 22V), cycle-by-cycle overcurrent protection, thermal shutdown protection
- Pb-free Packages,QFN3.5×4.5-20L

APPLICATIONS

- Wireless/ Speakers
- Portable Speakers
- Quick Charge Power Bank
- E-Cigarette
- Power Interface (USB Type-C, Thunderbolt)
- POS Terminal
- Tablet PC/Note Book

DESCRIPTION

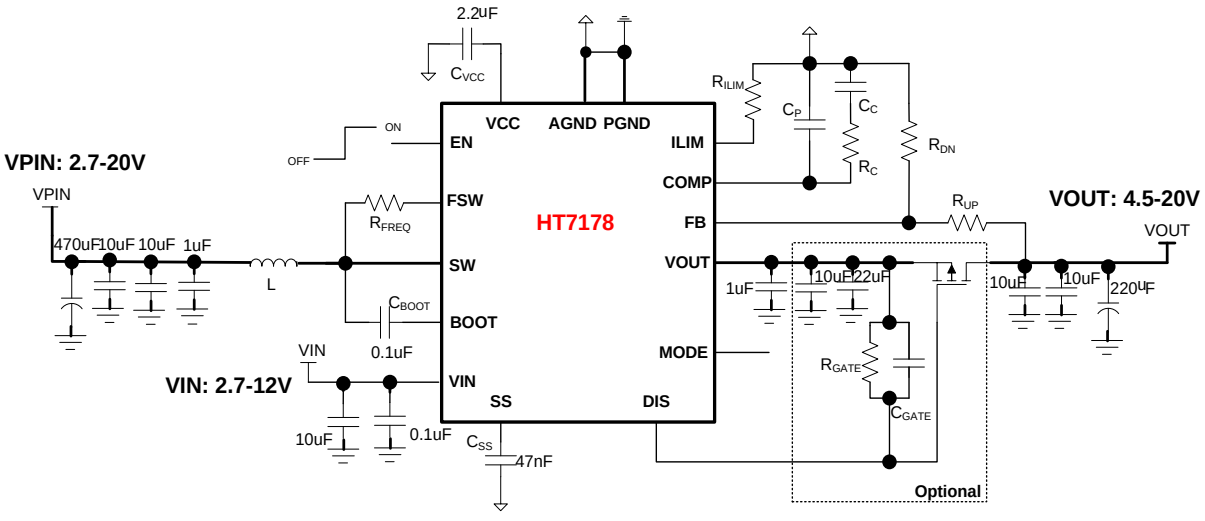
The HT7178 is a high-power density, fully integrated synchronous boost converter with a 16mΩ power switch and a 16mΩ rectifier switch to provide a high efficiency and small size solution in portable systems. The HT7178 has wide input voltage range from 2.7 V to 20 V to support applications with single cell, two cell Lithium batteries and 12V lead-acid batteries. The device has 14A switch current capability and can provide an output voltage up to 20V.

The HT7178 uses adaptive constant off-time peak current control topology to regulate the output voltage. In moderate to heavy load condition, it works in the PWM mode. In light load condition, the device has two operation modes selected by the MODE pin. One is PFM mode to improve the efficiency and another one is the forced PWM mode to avoid application problems caused by low switching frequency. The switching frequency in the PWM mode is adjustable ranging from 200kHz to 1.4MHz by an external resistor.

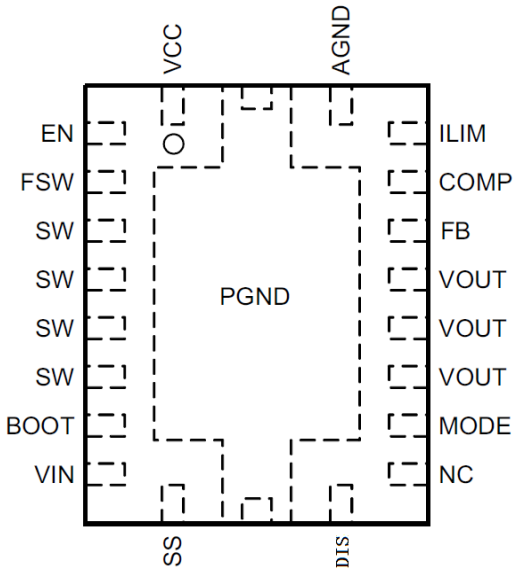
HT7178 could isolate the output from input side when shut down by a gate drive output disconnecting external FET, so that the load current consumption could be limited.

The HT7178 also implements a programmable soft-start function and an adjustable switching peak current limit function. In addition, the device provides 22V output overvoltage protection, cycle-by-cycle overcurrent protection, and thermal shutdown protection.

TYPICAL APPLICATION



■ TERMINAL CONFIGURATION



■ TERMINAL FUNCTION

Terminal No.	NAME	I/O[*1]	Description
1	VCC	O	Output of the internal regulator. A ceramic capacitor of 2.2uF is required between this pin and ground.
2	EN	I	Enable logic input. Logic high level enables the device. Logic low level disables the device and turns it into shutdown mode.
3	FSW	I	The switching frequency is programmed by a resister between this pin and the SW pin.
4/5/6/7	SW	PWR	The switching node pin of the converter.
8	BOOT	O	Power supply for high-side MOSTFET gate driver. A ceramic capacitor of 0.1μF must be connected between this pin and the SW pin.
9	VIN	I	IC power supply input.
10	SS	O	Soft-start programming pin. An external capacitor connected to ground sets the ramp rate of the internal error amplifier's reference voltage during soft-start
11	DIS	O	A gate drive output for the external disconnect FET. Connect the DISDRV pin to the gate of the external FET. Leave it floating if not using the load disconnect function.
12	NC	-	No connection inside the device. Connect these two pins to ground plane on the PCB for good thermal dissipation.
13	MODE	I	Operation mode selection pin for the device in light load condition. When this pin is connected to ground, the device works in PWM mode. When this pin is left floating, the device works in PFM mode.
14/15/16	VOUT	PWR	Boost converter output.
17	FB	I	Voltage feedback.
18	COMP	O	Output of the internal error amplifier, the loop compensation network should be connected between this pin and the AGND pin.
19	ILIM	I	Adjustable switch peak current limit. An external resister should be connected between this pin and the AGND pin.
20	AGND	-	Signal ground of the IC.
0	PGND	PWR	Power ground of the IC.

[1] I: input O: output PWR: power

■ ORDERING INFORMATION

Part Number	Package Type	Marking	Operating Temperature Range	Shipping Package / MOQ
HT7178DNER	QFN3.5×4.5-20L	HT7178	-40℃～85℃	Tape and Reel / 5000PCS

■ ELECTRICAL CHARACTERISTIC

● Absolute Maximum Ratings*2

PARAMETER		Symbol	MIN	MAX	UNIT
Voltage range	BOOT	/	-0.3	SW+7	V
	SW, FSW, V_{OUT}, DIS, V_{PIN}		-0.3	22.5	
	V_{IN}		-0.3	14	
	EN, VCC, SS, COMP, MODE		-0.3	7	
	ILIM, FB		-0.3	3.6	
Operating temperature range		T_A	-40	85	℃
Operating junction temperature range		T_J	-40	150	℃
Storage temperature range		T_{STG}	-50	150	℃

● Recommended Operating Conditions

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Input power voltage range	V_{PIN}		2.7		20	V
IC power supply voltage range	V_{IN}		2.7		12	V
Output voltage range	V_{OUT}		4.5		20	V
Inductance, effective value	L		0.47	2.2	10	μH
Input capacitance, effective value	C_I		10			μF
Output capacitance, effective value	C_O		6.8	47	1000	μF
Operating temperature	T_a		-40	25	85	℃
Operating junction temperature	T_J		-40		125	℃

[2] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

Electrical Characteristics[3]

Condition: Ta = 25ºC, V_{PIN} = 2.7V-20V, V_{OUT}=4.5-20V, unless otherwise specified.

Power Supply

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Input power voltage range	V_{PIN}		2.7		20	V
IC power supply voltage range	V_{IN}		2.7		12	V
Under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	VIN rising			2.7	V
		VIN falling			2.5	V
VIN UVLO hysteresis	V_{IN_HYS}			200		mV
VCC UVLO threshold	V_{CC_UVLO}			2.1		V
Operating quiescent current from V_{PIN} + V_{IN}	I_Q	V_{IN} =V_{PIN} = 3.3V, V_{OUT} = 7.5V		600		uA
		V_{IN} =V_{PIN} = 7.2V, V_{OUT} = 12V		390		
		V_{IN} =V_{PIN} = 12V, V_{OUT} = 18V		460		
Shutdown current into V_{PIN} + V_{IN}	I_{SD}	IC disabled, V_{IN} =V_{PIN} = 3.6 V		1		uA
		IC disabled, V_{IN} =V_{PIN} = 7.4 V		4		
VCC regulation	V_{CC}			5.2		V

EN and Mode Input

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
EN high threshold voltage	V_{ENH}		1.5			V
EN low threshold voltage	V_{ENL}				0.4	V
EN internal pull-down resistance	R_{EN}			800		kΩ
MODE high threshold voltage	V_{MODEH}		4			V
MODE low threshold voltage	V_{MODEL}				1.5	V
MODE internal pull-up resistance	R_{MODE}			800		kΩ

OUTPUT

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Output voltage range	V_{OUT}	Freq = 500 kHz	4.5		20	V
Output overvoltage protection	V_{OVP}		21.5	22	22.5	V
Reference voltage at the FB pin	V_{REF}		1.186	1.204	1.222	V
Soft-start charging current	I_{SS}			5		uA

ERROR AMPLIFIER

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
COMP pin sink current	I_{SINK}	V_{FB} = V_{REF} +200 mV, V_{COMP} = 1.5 V		20		uA
COMP pin source current	I_{SOURCE}	V_{FB} = V_{REF} –200 mV, V_{COMP} = 1.5 V		20		uA
High clamp voltage at the COMP pin	V_{CC_LPH}	V_{FB} = 1 V, R_{ILIM} = 100 kΩ		2.3		V
Low clamp voltage at the COMP pin	V_{CC_LPL}	V_{FB} = 1.5 V, R_{ILIM} = 100 kΩ,		1.4		V
Error amplifier transconductance	G_{EA}	V_{COMP} = 1.5 V		190		uA/V

[3] Depending on parts and pattern layout, characteristics may be changed

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
POWER SWITCH						
MOSFET on-resistance	$R_{DS(on)}$	High-side MOSFET		16		mΩ
		Low-side MOSFET		16		mΩ
CURRENT LIMIT						
Peak switch current limit	I_{LIM}	R_{ILIM} = 100 kΩ,	11	12	13	A
		R_{ILIM} = 82 kΩ,	13	14	15	
Reference voltage at the ILIM pin	V_{ILIM}			1.204		V
SWITCHING FREQUENCY						
Switching frequency	f_{SW}	R_{FREQ} = 220 kΩ, V_{PIN} = 3.6V, V_{OUT} = 12V		600		kHz
Minimum on-time	t_{ON_min}	R_{FREQ} = 220 kΩ, V_{PIN} = 3.6V, V_{OUT} = 12V		90	180	ns
GATE DRIVER FOR LOAD DISCONNECT						
Driver current for the external FET	I_{GD_SINK}			55		uA
THERMAL SHUTDOWN						
Thermal shutdown threshold	T_{SD}			150		℃
Thermal shutdown hysteresis	T_{SD_HYS}			20		℃

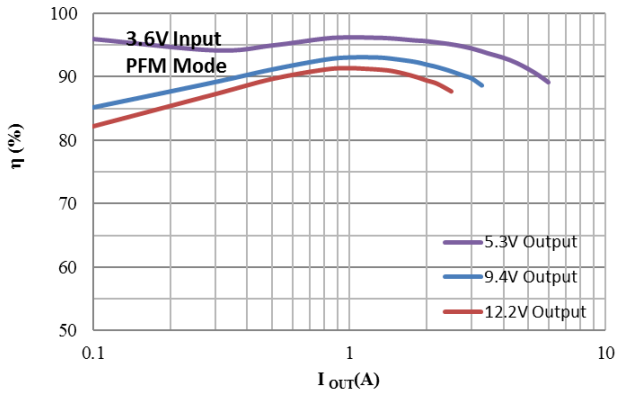
- **Voltage Setting Reference for HT7178**

Input Power	Referred Max Input Current (RMS Value)	Input Voltage	Output Voltage	Referred Max Output Current (RMS Value)	Output Power	Efficiency	Pull-up resistor from FB	Pull-down resistor from FB
P_{PIN} (W)	I_{PIN}(A)	V_{PIN}(V)	V_{OUT}(V)	I_{OUT}(A)	P_{OUT} (W)	η(%)	R_{UP}(Ω)	R_{DN}(Ω)
33.30	9.0	3.7	7.3	4.0	29.20	87.7%	510k	100k
35.15	9.5	3.7	9.4	3.3	31.02	88.3%	510k	75k
34.78	9.4	3.7	12.2	2.5	30.50	87.7%	510k	56k
68.08	9.2	7.4	12.2	5.2	63.44	93.2%	510k	56k
67.86	9.2	7.4	15.5	4.0	62.00	91.4%	510k	43k
74.00	10.0	7.4	18.3	3.6	65.88	89.0%	510k	36k
117.48	9.8	12	18.3	6.0	109.80	93.5%	510k	36k
124.80	10.4	12	19.5	6.0	117.00	93.8%	510k	33k

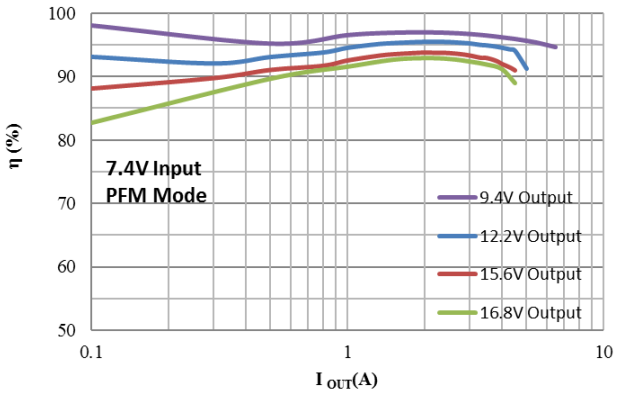
■ TYPICAL OPERATING CHARACTERISTICS

Condition: L = 1.5uH, R_{ILIM} = 82k， R_{FREQ} = 200k, Output Capacitor = 1uF//10uF//10uF//220uF, PFM mode, otherwise specified.

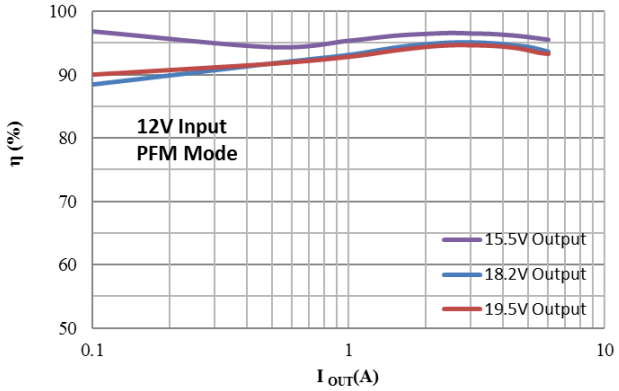
I_{OUT} vs η



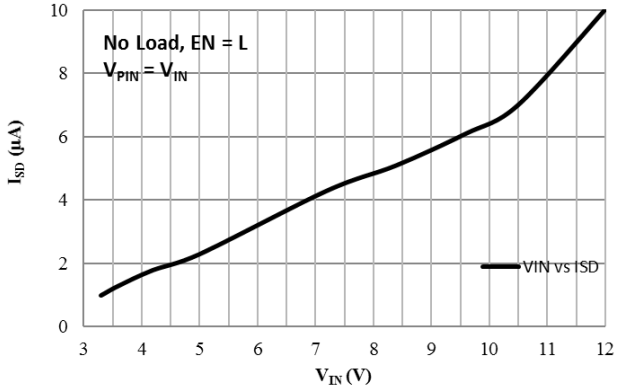
I_{OUT} vs η



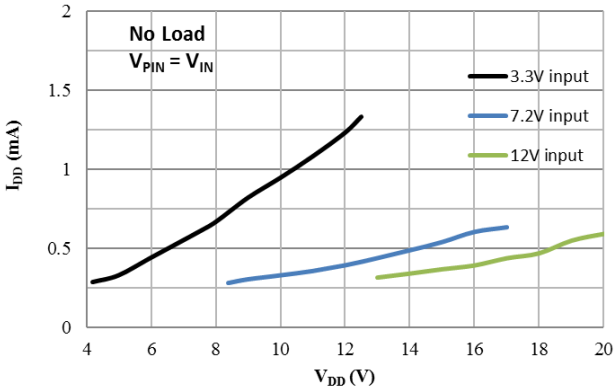
I_{OUT} vs η

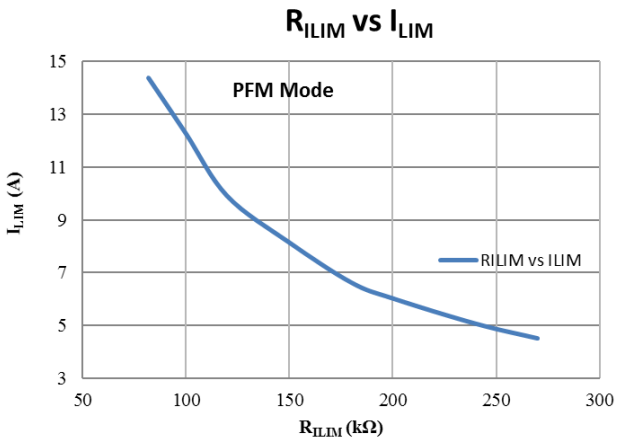


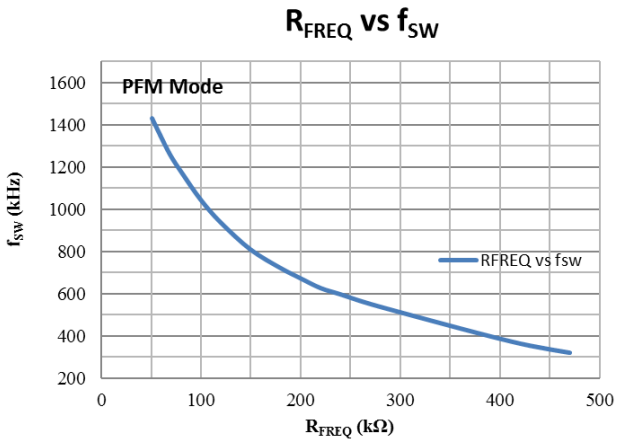
V_{IN} vs I_{SD}



V_{IN} vs I_Q

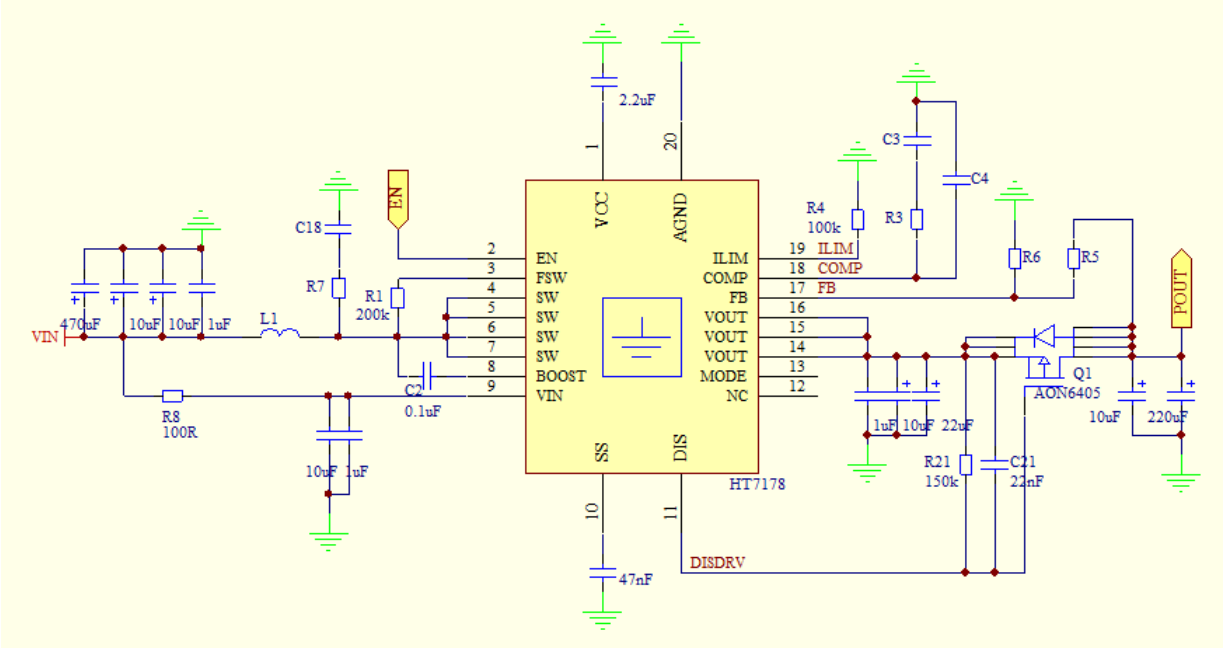



R_{ILIM} vs I_{LIM}
PFM Mode
RILIM vs ILIM
I_{LIM} (A)
15
13
11
9
7
5
3
50
100
150
200
250
300
R_{ILIM} (kΩ)


R_{FREQ} vs f_{SW}
PFM Mode
RFREQ vs fsw
f_{SW} (kHz)
1600
1400
1200
1000
800
600
400
200
0
100
200
300
400
500
R_{FREQ} (kΩ)

■ APPLICATION INFORMATION

1. Typical Application



Do make sure that the voltage peak of pin V_{IN} should be lower than 12V. If the input power voltage is higher than 12V (V_{PIN} > 12V), use a 3.3V or 5V logic power supply to connect V_{IN} or use a lager resistor connecting between V_{PIN} and V_{IN}.

2. Feature Description

2.1. Functional Modes (Mode pin)

Operation

The synchronous boost converter HT7178 operates at a quasi-constant frequency pulse width modulation (PWM) in moderate to heavy load condition. Based on the V_{PIN} to V_{OUT} ratio, a circuit predicts the required off-time of the switching cycle. At the beginning of each switching cycle, the low-side N-MOSFET switch is turned on, and the inductor current ramps up to a peak current that is determined by the output of the internal error amplifier. After the peak current is reached, the current comparator trips, and it turns off the low-side N-MOSFET switch and the inductor current goes through the body diode of the high-side N-MOSFET in a dead-time duration. After the dead-time duration, the high-side N-MOSFET switch is turned on. Because the output voltage is higher than the input voltage, the inductor current decreases. The high-side switch is not turned off until the fixed off-time is reached. After a short dead-time duration, the low-side switch turns on again and the switching cycle is repeated.

In light load condition, the HT7178 implements two operation modes, PFM mode and forced PWM mode, to meet different application requirements. The operation mode is set by the status of the MODE pin. When the MODE pin is connected to ground, the device works in the forced PWM mode. When the MODE pin is left floating, the device works in the PFM mode, which is the recommended mode.

PWM Mode

In the forced PWM mode, the HT7178 keeps the switching frequency unchanged in light load condition. When the load current decreases, the output of the internal error amplifier decreases as well to keep the inductor peak current down, delivering less power from input to output. When the output current further reduces, the current through the inductor will decrease to zero during the off-time. The high-side N-MOSFET is not turned off even if the current through the MOSFET is zero. Thus, the inductor current changes its direction after it runs to zero. The power flow is from output side to input side. The efficiency will be low in this mode. But with the fixed switching frequency, there is no audible noise and other problems which might be caused by low switching frequency in light load condition.

PFM Mode

The HT7178 improves the efficiency at light load with the PFM mode. When the converter operates in light load condition, the output of the internal error amplifier decreases to make the inductor peak current down, delivering less power to the load. When the output current further reduces, the current through the inductor will decrease to zero during the off-time. Once the current through the high side N-MOSFET is zero, the high-side MOSFET is turned off until the beginning of the next switching cycle. When the output of the error amplifier continuously goes down and reaches a threshold with respect to the peak current of ILIM / 12, the output of the error amplifier is clamped at this value and does not decrease any more. If the load current is smaller than what the HT7178 delivers, the output voltage increases above the nominal setting output voltage. The HT7178 extends its off time of the switching period to deliver less energy to the output and regulate the output voltage to 0.7% higher than the nominal setting voltage. With the PFM operation mode, the HT7178 keeps the efficiency above 80% even when the load current decreases to 1 mA. In addition, the output voltage ripple is much smaller at light load due to low peak current.

2.2. Enable and Startup (EN and SS pin)

The HT7178 has an adjustable soft start function to prevent high inrush current during start-up. To minimize the inrush current during start-up, an external capacitor, connected to the SS pin and charged with a constant current, is used to slowly ramp up the internal positive input of the error amplifier. The larger the capacitance at the SS pin, the slower the ramp of the output voltage and the longer the soft-start time. A 47-nF capacitor is usually sufficient for most applications.

When the EN pin is pulled into logic low (below 0.4V), the HT7178 goes into the shutdown mode and stops switching. Only when EN pin is pulled into logic high (above 1.5V), the HT7178 works.

2.3. Adjustable Switching Frequency (FSW pin)

This device features a wide adjustable switching frequency ranging from 200 kHz to 1.4MHz. The switching frequency is set by a resistor (R_{FREQ}) connected between the FSW pin and the SW pin of the HT7178. R_{FREQ} must always be connected from the FSW pin to SW pin for proper operation. R_{FREQ} can be calculated by:

$$R_{FREQ} = \frac{4 \times (\frac{1}{f_{SW}} - t_{DELAY} \times \frac{V_{OUT}}{V_{PIN}})}{C_{FREQ}}$$

where

- R_{FREQ} is the resistance connected between the FSW pin and the SW pin.
- C_{FREQ} = 23pF.
- f_{SW} is the desired switching frequency.
- t_{DELAY} = 89 ns.
- V_{PIN} is the input voltage.
- V_{OUT} is the output voltage.

NOTE: A resistor value of 180-300k is recommended for R_{FREQ} to get a f_{SW} of around 450-700kHz.

2.4. Load Disconnect Gate Driver (DIS pin)

The HT7178 provides a DIS pin to drive the external FET at the output side, which completely disconnects the output from the input end during shutdown or output short happens. During the device's start-up phase, the disconnect FET is controlled by the gate driver voltage of the external disconnect FET, there is an internal 55μA (typical) sink current. The load disconnect FET connection is shown as Figure 1. Do make sure that C_{OUT2} should be no larger than 10 x C_{OUT1} to avoid the inrush current when turning on the disconnect FET.

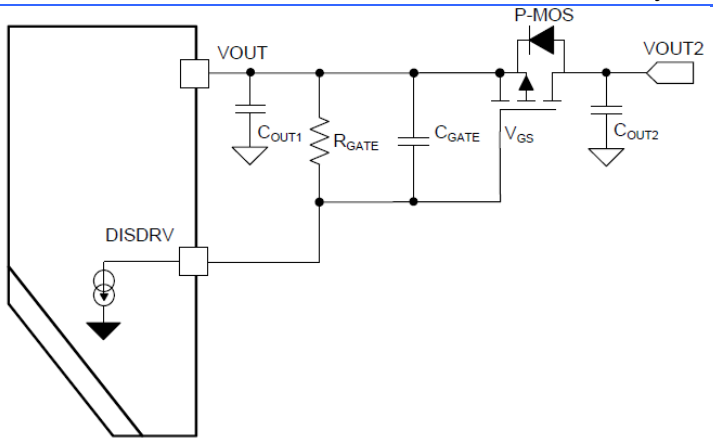


Figure 1 Load Disconnect FET Connection

The FET parameter should be considered as follows:

- The drain-to-source voltage rating V_{DS} should be higher than the output max. voltage V_{OUT}.
- The drain-to-source RMS current rating I_{DS}(RMS) should be higher than the maximum output current.

The driver voltage and turn on / off timing can be set via the resistor R_{GATE} and capacitor C_{GATE} connecting between with the DIS pin and the source of the external FET. 150K and 22nF can be used in most cases.

To set the C_{GATE}, the following equation can be used:

$$C_{GATE} \approx C_{GS\_PFET} = \frac{T_{ON\_PFET} \times I_{DIS\_PFET}}{V_{TH\_PFET}}$$

where

- C_{GS_PFET} is the total gate capacitance of connected between gate and source external FET. (including the self-gate-source capacitance of the FET). The maximum capacitance C_{GS_PFET} should be < 100nF.
- T_{ON_PFET} is the turn on time of external FET. The max T_{ON_PFET} should not exceed 3ms
- I_{DIS_PFET} is the discharge current inside of HT7178, it is 55μA typically.
- V_{TH_PFET} is the gate threshold of external FET.

To set the R_{GATE}, the following equation can be used:

$$R_{GATE} = \frac{V_{GATE}}{I_{DIS\_PFET}}$$

While DIS is not used, it can be connected to GND so that a more integral GND plane can be achieved to decrease the loop of output peak current.

2.5. Adjustable Peak Current Limit (ILIM pin)

To avoid an accidental large peak current, an internal cycle-by-cycle current limit is adopted. The low-side switch is turned off immediately as soon as the switch current touches the limit. The peak switch current limit can be set by a resistor (R_{ILIM}) at the ILIM pin to ground. The relationship between the current limit and the resistance is as follows:

$$I_{LIM} = \frac{1200000}{R_{ILIM}}$$

2.6. Output Voltage Setting (FB pin)

The output voltage is set by an external resistor divider (R_{UP}, R_{DN} in the Typical Application Circuit). To get the output voltage V_{OUT}, the Value of R_{UP} and R_{DN} can be calculated as:

$$V_{OUT} = V_{REF} \times (1 + \frac{R_{UP}}{R_{DN}})$$

Where V_{REF} = 1.204V.

Some typical output voltages can be set as the following parameters.

V_{OUT}(V)	R_{UP}(Ω)	R_{DN}(Ω)
9.4	510k	75k
12.2	510k	56k
15.5	510k	43k
18.3	510k	36k

2.7. Inductor Selection (SW pin)

Because the selection of the inductor affects the power supply's steady state operation, transient behavior, loop stability, and boost converter efficiency, the inductor is the most important component in switching power regulator design. Three most important specifications to the performance of the inductor are the inductor value, DC resistance, and saturation current.

To be simplified, the inductor value can be set as 2.2uH which can be used in most cases.

The rated current, especially the saturation current should be larger than the peak current during the whole operation. The peak current can be calculated as follows.

$$I_{Lpeak} = I_{DC} + \frac{I_{PP}}{2}$$

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta}$$

$$I_{PP} = \frac{1}{L \times (\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}}) \times f_{SW}}$$

Boost converter efficiency is affected significantly by the inductor's DC resistance (DCR), equivalent series resistance (ESR) at the switching frequency, and the core loss. An inductor with lower DCR and ESR would increase the efficiency significantly.

The inductor should be placed as close as possible to the SW pin. For a lower EMI radiation, connecting a resistor and a capacitor in series to the ground would be helpful. 1ohm resistor and 10nF capacitor would be recommended in most cases.

2.8. Input Capacitor Selection (V_{IN}, V_{PIN}, VCC pin)

For good input voltage filtering and small voltage ripple (less than 100mV is required), we recommend low-ESR capacitors of 1uF//10uF//10uF//470uF ("//" represents paralleled) be placed as close as possible to the inductor.

The V_{IN} pin is the power supply for the HT7178, a 1uF paralleled with 10uF ceramic capacitor should be placed as close as possible to the V_{IN} pin. Notice that the maximum voltage of V_{IN} should be lower than 12V, so if V_{IN} is supplied from V_{PIN}, a resistor of 10R is required between input power supply V_{PIN} and V_{IN} pin so that the power supply of HT7178 would be more stable, and if V_{PIN} is larger than 12V, the value of the resistor should be higher to get a lower voltage of V_{IN}. An extensive power supply such as the logic power supply connecting to V_{IN} would be another choice. Be aware of that the current consumption of V_{IN} is lower than 10mA.

The VCC pin is the output of internal LDO. A ceramic capacitor of 2.2uF is required at the VCC pin to get a

stable operation of LDO.

2.9. Output Capacitor Selection (V_{OUT} pin)

To be simplified, we recommend low-ESR capacitors of 1uF//10uF//10uF//470uF ("//" represents paralleled) be placed as close as possible to VOUT pin for small output voltage ripple.

Capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance.

In detail, for the require output voltage ripple, use the following equations to calculate the minimum required effective capacitance C_{OUT}

$$V_{ripple\_dis} = \frac{(V_{OUT} - V_{PIN_{MIN}}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times C_{OUT}}$$

$$V_{ripple\_ESR} = I_{Lpeak} \times R_{C\_ESR}$$

Where

- V_{ripple_dis} is output voltage ripple caused by charging and discharging of the output capacitor.
- V_{ripple_ESR} is output voltage ripple caused by ESR of the output capacitor.
- V_{PIN_MIN} is the minimum input voltage of boost converter..
- V_{OUT} is the output voltage..
- I_{OUT} is the output current.
- I_{Lpeak} is the peak current of the inductor.
- f_{SW} is the converter switching frequency.
- R_{C_ESR} is the ESR of the output capacitors.

2.10. Loop Stability (COMP pin)

The HT7178 requires external compensation, which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external compensation network comprised of resister R_C, ceramic capacitors C_C and C_P is connected to the COMP pin.

To be simplified, R_C is 56kΩ, C_C is 3.3nF, and C_P can be floating. But notice that this setting can only be adopted in most cases. In detail, the compensation network parameters can be calculated as follows.

(1) Set the cross over frequency, f_c

The first step is to set the loop crossover frequency, f_C. The higher crossover frequency, the faster the loop response is. It is generally accepted that the loop gain cross over no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{RHPZ}. It's proper to use a fixed parameter of 10kHz for f_C.

$$f_{RHPZ} = \frac{R_O \times (1-D)^2}{2\pi \times L}$$

(2) Set the compensation resistor, R_C.

$$R_C = \frac{2\pi \times V_{OUT} \times R_{sense} \times f_C \times C_O}{(1-D) \times V_{REF} \times G_{EA}}$$

(3) Set the compensation zero capacitor, C_C

$$C_C = \frac{R_O \times C_O}{2 \times R_C}$$

(4) Set the compensation pole capacitor, C_P

$$C_P = \frac{R_{ESR} \times C_O}{R_C}$$

If the C_P is less than 10pF, it can be left open.

- R_O is the output load resistance.
- D is the switching duty cycle. 1 - D = V_{PIN} / V_{OUT}
- R_{sense} is the equivalent internal current sense resistor, which is 0.084 Ω.
- C_O is output capacitor.
- V_{REF} is the reference voltage at the FB pin, which is 1.204V.
- G_{EA} is the amplifier's transconductance, which is 190uA/V.
- R_{ESR} is the equivalent series resistance of the output capacitor.

2.11. Selecting the Bootstrap Capacitor (BOOT pin)

The bootstrap capacitor (C_{BST}) between the BOOT and SW pin supplies the gate current to charge the high-side FET device gate during each cycle's turn-on and supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is 0.1μF to 1μF. C_{BST} should be a good quality, low ESR, ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of 0.1μF can be used in most cases.

2.12. Protection Function

Under-voltage Lockout (UVLO)

The UVLO circuit prevents the device from malfunctioning at low input voltage and the battery from excessive discharge. The HT7178 has both V_{IN} UVLO function and VCC UVLO function. It disables the device from switching when the falling voltage at the V_{IN} pin trips the UVLO threshold V_{IN_UVLO}, which is typically 2.4V. The device starts operating when the rising voltage at the VIN pin is 200mV above the V_{IN_UVLO}. It also disables the device when the falling voltage at the VCC pin trips the UVLO threshold V_{CC_UVLO}, which is typically 2.1V.

Over-voltage Protection

If the output voltage at the VOUT pin is detected above 22 V (typical value), the HT7178 stops switching immediately until the voltage at the VOUT pin drops the hysteresis value lower than the output overvoltage protection threshold. This function prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

Thermal Shutdown

A thermal shutdown is implemented to prevent damages due to excessive heat and power dissipation. Typically, the thermal shutdown happens at a junction temperature of 150°C. When the thermal shutdown is triggered, the device stops switching until the junction temperature falls below typically 130°C, then the device starts switching again.

3. Application Notes

3.1. Radiated EMI Reduction

(1) Minimize High di/dt Path Loop Area

EMI Starts off from high di/dt loops. The high di/dt critical path locates as the red circle showed in the following figure. The output capacitor should be placed as close to the VOUT pin as possible resulting in minimum area of the high di/dt loop.

The DIS pin (when not used) and NC pin can be connected to PGND ground plane which is good for thermal dissipation, can reduce the impedance of the return path and make the placement of the output capacitors easier.

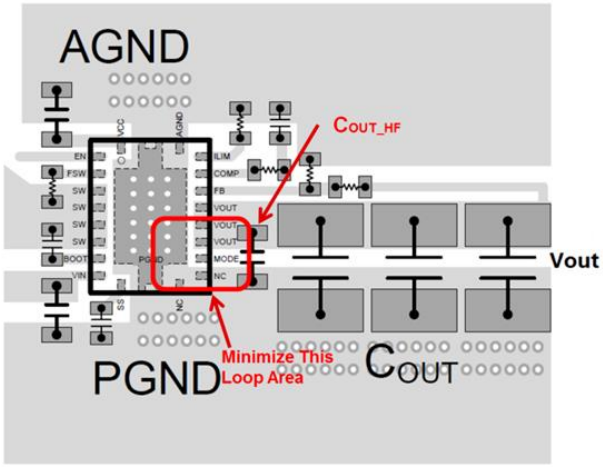


Figure 2 Critical Path Layout

(2) PCB Trace and Ground Plane

High trace inductance leads to poor radiation EMI. The inductance of a PCB trance is a function of its length and width. So, increase the trace width and decrease the trace length will significantly decrease the radiation EMI.

Meanwhile, good designed ground planes will help decrease the radiation EMI too:

- Placing a solid ground plane with minimum distance to the critical trace;
- Wider and bigger ground plane result in smaller signal trace inductance;
- Thinner insulation thickness between the ground plane and the signal traces also results in smaller inductance;

(3) RC Snubber

Adding an RC snubber across the SW pin and the power ground can help reduce the radiation EMI levels. The RC snubber should be placed as close as possible to the switching node and the power ground.

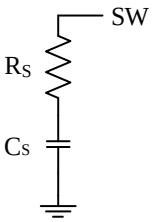


Figure 3 Placement of RC Snubber

The aim of the snubber resistor RS is to add sufficient damping to the parasitic resonant circuit. The value of R_S depends on the desired damping factor and the parasitic inductor I_P and parasitic capacitor C_P of the circuit:

$$R_S = \frac{1}{\xi} \times \sqrt{\frac{L_P}{C_P}}$$

Where ξ is the damping factor, normally can range from 0.5 to 1.

The value of L_P and C_P can be measured by:

- Measure the original ringing frequency $f_{RING;}$
- Add some small capacitance from switch node to ground. Keep increasing capacitance until the ringing frequency is 50% of the original ringing frequency f_{RING}, and the capacitance is C_S, C_P = 1/(3C_S);
- $L_P = \frac{1}{C_P \times (2\pi \times f_{RING})^2}$

To be simplified, a resistor of 1ohm (R_S) and a capacitor of 2.2nF (C_S) can be used. However, notice that larger C_S results in higher power loss.

(4) Radiation from Cables

A longer input or output cables result in poor radiation EMI. So, make the length of input cable and output cable very close to the real application.

(5) Ferrite Bead

Ferrite Bead is used in series with the power line. Before using a ferrite bead, you need to consider about the specifications of the bead as follows:

- The frequency characteristics

Make sure that the resistive impedance of the bead is much higher than the reactive impedance in the noise frequency range.

- The rated current

Make sure that the rated current of the bead should be at least 30% higher than the expected maximum current.

- The DC resistance

The DC resistance of the ferrite bead should be as low as possible.

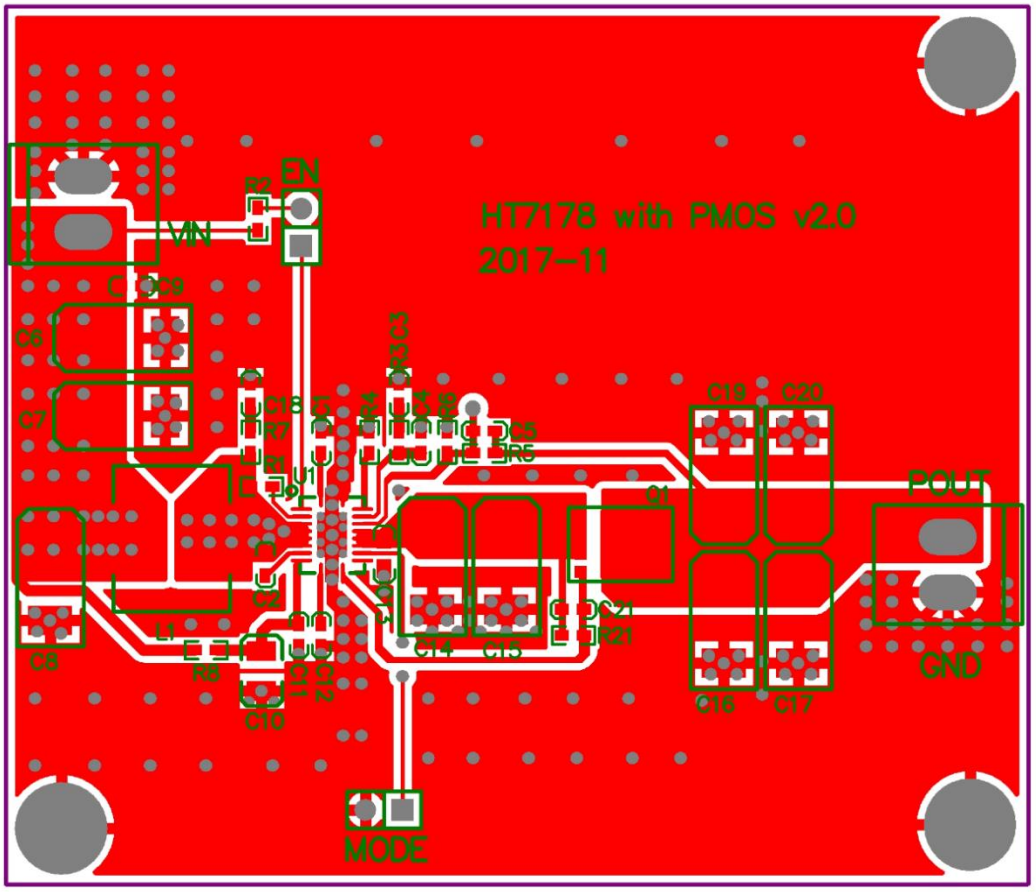
3.2. Layout Guidelines

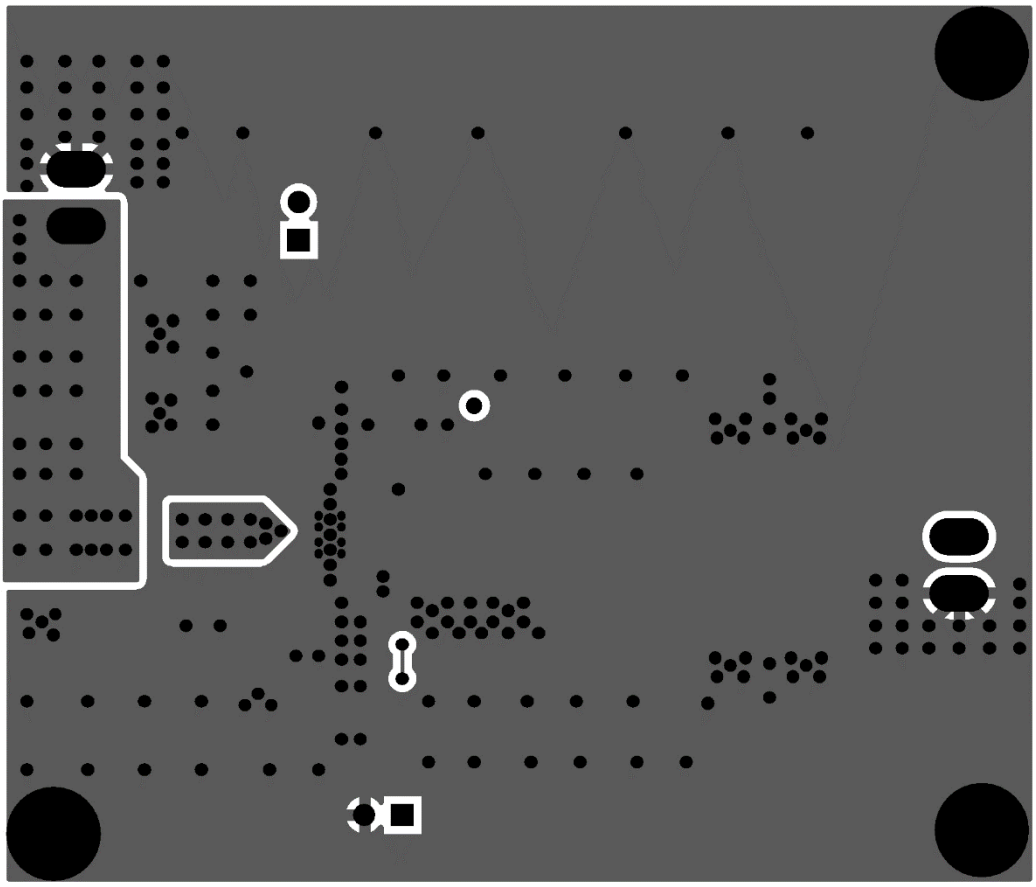
As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability and noise problems. To maximize efficiency, switch rise and fall times are very fast. To prevent radiation of high frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling.

The input capacitor needs to be close to inductor L, the V_{IN} pin and GND pin in order to reduce the input supply ripple. The output capacitor needs to be close to V_{OUT} pin and GND pin in order to reduce the output supply ripple.

The layout should also be done with well consideration of the thermal as this is a high-power density device. A thermal pad that improves the thermal capabilities of the package should be soldered to the large ground plate, using thermal vias underneath the thermal pad.

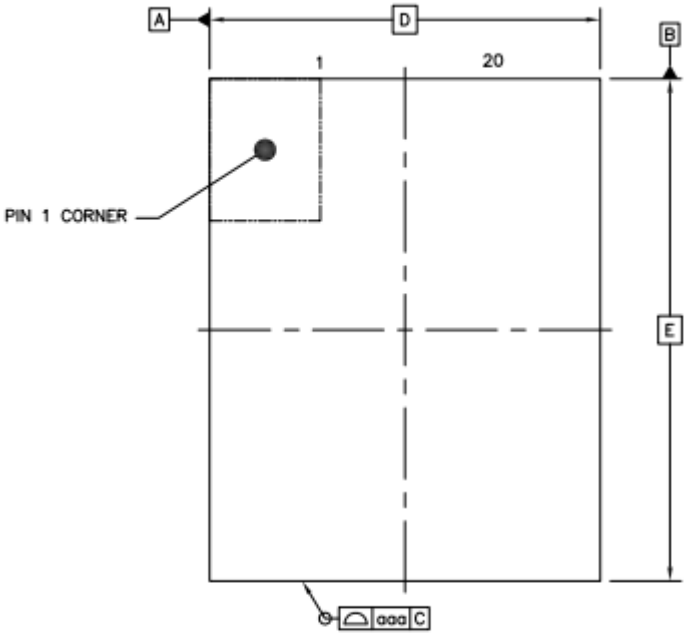
3.3. Layout Examples



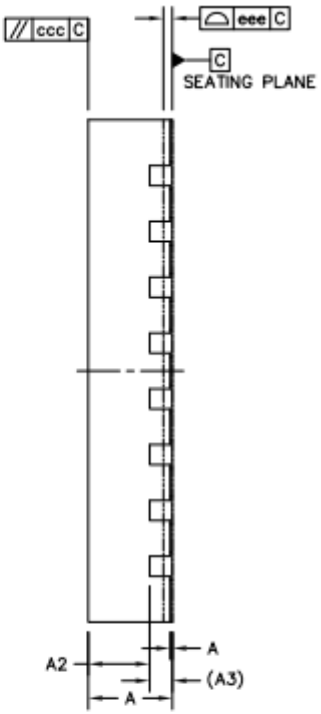


■ PACKAGE OUTLINE

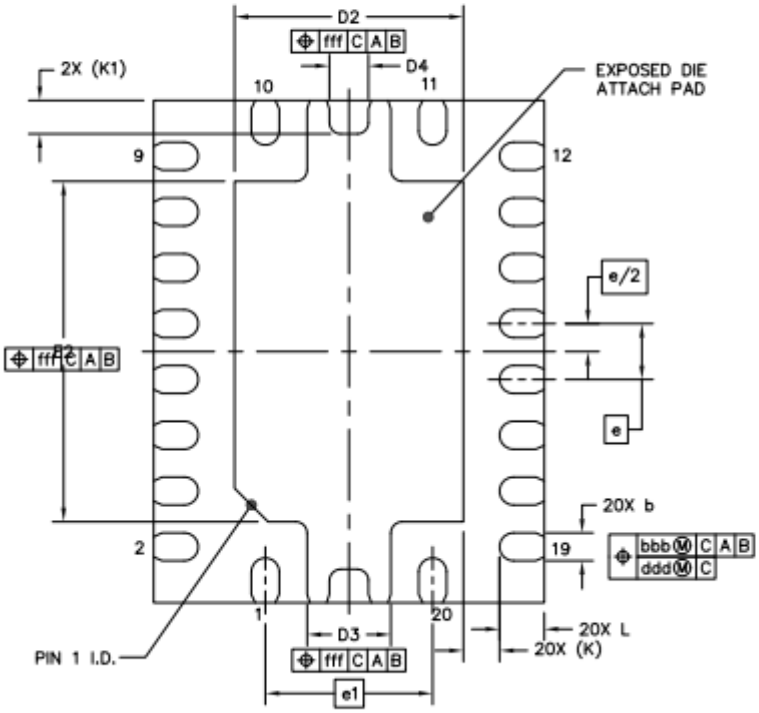
DNE (QFN3.5×4.5-20L), Unit: mm



TOP VIEW



SIDE VIEW



BOTTOM VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		3.5 BSC	
	Y	E		4.5 BSC	
LEAD PITCH		e		0.5 BSC	
LEAD PITCH		e1		1.5 BSC	
EP SIZE	X	D2	1.95	2.05	2.15
	Y	E2	2.95	3.05	3.15
	X	D3	0.65	0.75	0.85
EP EDGE TO EP EDGE		D4	0.25	0.35	0.45
LEAD LENGTH		L	0.3	0.4	0.5
EP EDGE TO PACKAGE EDGE		K1		0.3 REF	
LEAD TIP TO EXPOSED PAD EDGE		K		0.325 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	

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