15W Wireless Power Transmitter SOC

Description

The OPS1033 is a highly integrated, magnetic induction, wireless power transmitter supporting the WPC1.3 specifications. The product is designed to operate with a wide input supply voltage range of 4.5V to 20V. The system-on-chip device is comprised of a step-down switching regulator, linear regulators, a microcontroller, Q factor detector，voltage and current ASK decoders, Two-Half bridge power stages drivers and 4-power MOSFETs.

The OPS1033 support PD 3.0 protocol for PD adapter, which can be adjusted the input supply voltage. And support Qualcomm Quick Charge technology when using a QC2.0 or QC3.0 power adaptor.

The OPS1033 includes an industry-leading 32-bit MCU processor offering a high level of programmability while consuming extremely low standby power less than 10uA. It can provide Automatic wake up function with the ability which can calculate Q factor under battery voltage. OPS1033 has excellent thermal performance due to high efficiency driver and integrated MOSFET low Rdson. In addition, the microcontroller empowers the user to customize features such as LED patterns, buzzer, and FOD threshold settings. The SWD or I^2C serial communication allows the user to read information such as voltage, current, frequency, and fault conditions.

The OPS1033 includes an under-voltage lockout and thermal management circuit to safeguard the device under fault conditions. Together with the Crechip OPS1121A/B, the OPS1033 offers a complete wireless power system solution.

The OPS1033 is available in a lead-free, space-saving QFN34-5x5x0.75mm package. The product is rated for a -40℃ to +85℃ operating temperature range.

Features

- WPC1.3 compliant, flexible coil configuration
- Wide input voltage range: 4.5V to 20V
- Efficient 5W/7.5W/10W/15W/20W power transfer with typical 85% efficiency at 10W output
- Supports quick charging power adaptors of USB PD3.0, QC 2.0/3.0 etc.
- Integrated step-down switching regulator, linear regulator, 2-half bridge drivers and 4-power MOSFETs
- Low standby power consumption (<10uA)
- Dedicated remote temperature sensing(NTC)
- Supports 127.7KHz fixed frequency and voltage tuning by PD3.0 protocols or off-chip DCDC
- Supports WPC EPP Q detection or advanced proprietary Q detection with programmable FOD sensitivity
- Embedded 32bit core microprocessor
- Supports over-voltage, over-current, over-temperature detection and protection
- Supports I^2C interface for program/debug/control
- User-programmable power transfer LED indicators
- 5mm x 5mm x0.75mm, pitch 0.4mm, QFN 34pin package

Typical Applications

- BPP and EPP Wireless Charging Pads
- Up to 7.5W/15W/20W charging for iPhones

- After-Market Automotive Wireless Charging
- Portable Instruments/ Electronic Equipment
- Charging Cradles

Description for Implementation

1. Overview and function

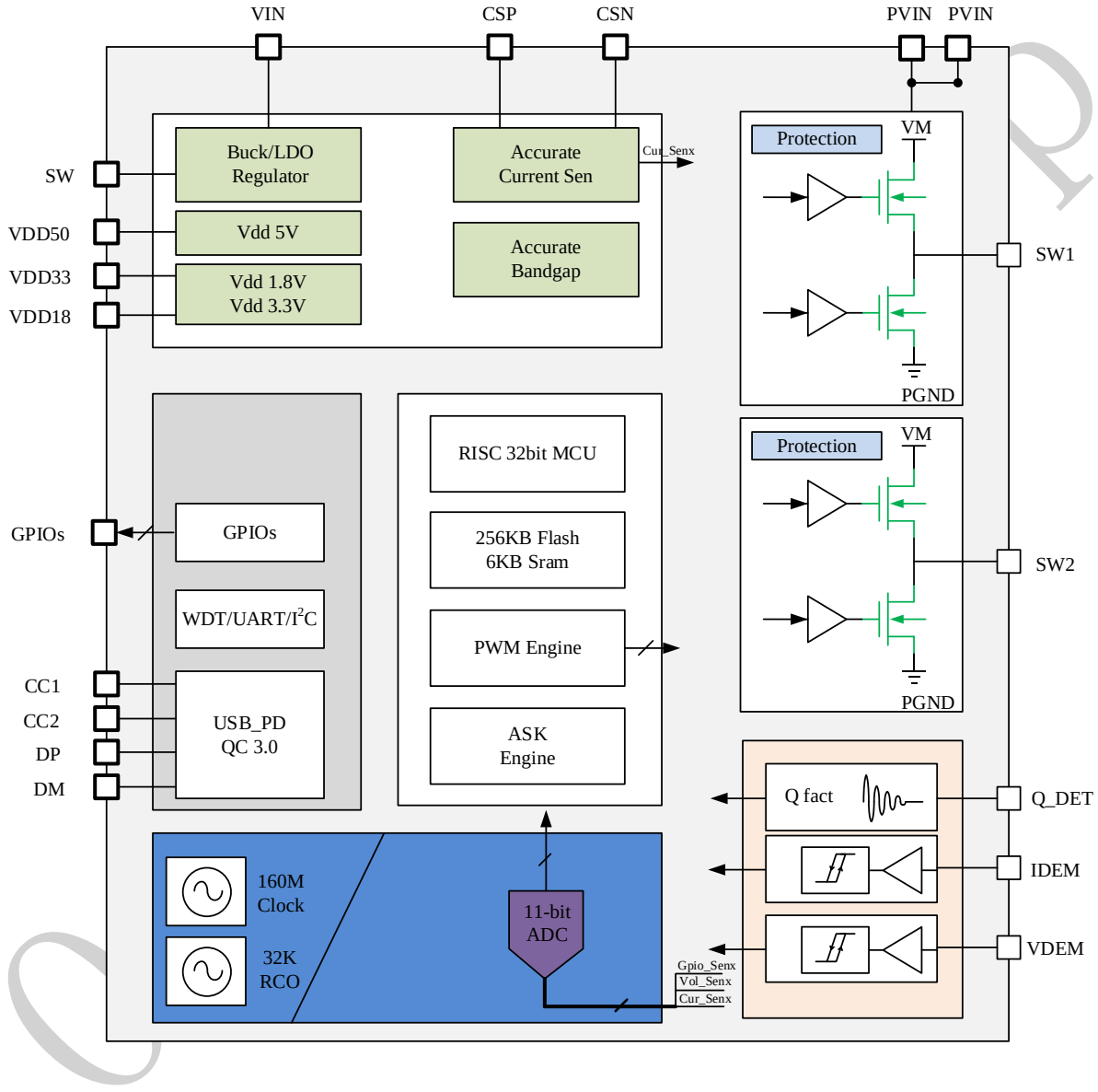


Figure 1 OPS1033 function block diagram

Figure 1 is the function block diagram of OPS1033 which is compliant with QI 1.3 and supports 5W/7.5W/10W/15W/20W transmission power. The efficient buck can work stably with input voltage from 4.5V to 20V and be bypassed when it is below the working voltage. It can automatically change the PFM and PWM modulation according to the load condition which can get best efficiency in different conditions.

The OPS1033 high voltage drivers change DC power to AC power with integrated MOSFETs. Each PWM's frequency and duty cycle can be configured independently from 110KHz to 200KHz frequency output. High

resolution PLL can realize 1Hz frequency step and 0.1% duty PWM resolution. Q factor detector is the key feature which can realize the object detection, FOD detection and low standby power operation.

The Chip realizes the communication with the receiver through ASK and FSK modulation. It supports voltage and current ASK demodulation without any external active device. The patented demodulation algorithm can ensure the charging stability under various interferences and different positions. The high speed PWM clock guarantees that the difference between FSK reference frequency and modulation frequency conforms to QI EPP standard.

The OPS1033 supports internal voltage, current, temperature detection and abnormal protection. External NTC protection can be used to ensure chip charging safety. Two LED outputs are used to indicate charging status and abnormal protection. FOD sensitivity can be programmed according to user's requirement.

2. Pin Definition and Descriptions

2.1 Pin Definition

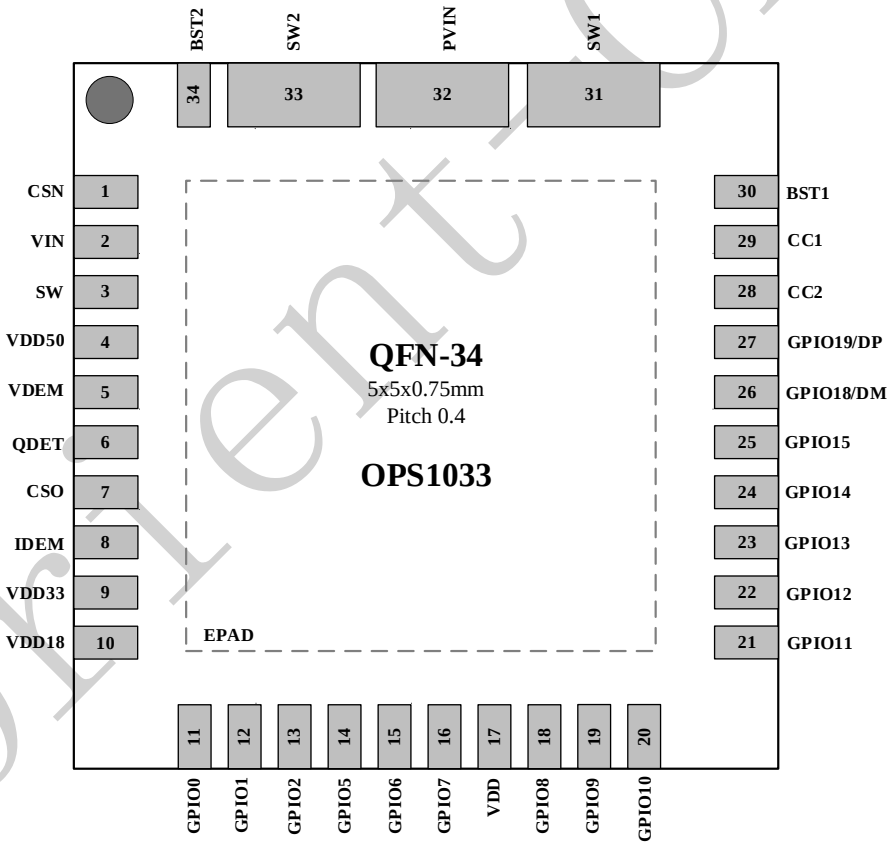


Figure 2 OPS1033 Pin Definition (QFN34-5x5x0.75mm, pitch 0.4mm)

2.2 Pin Description

ORDER	NAME	I/O TYPE	DESCRIPTION
1	CSN	AI(HV)	Current Sense Negative terminal connect
2	VIN	PI(HV)	Input voltage for HV analog. Bypass with a 10μF and 0.1μF ceramic capacitor to GND
3	SW	AIO(HV)	Internal step-down regulator's switch node. Connect an external 4.7μH inductor to this pin.
4	VDD50	PI(5.0V)	5V supply input power supply. Connect this pin to the 5V output of the step-down regulator.
5	VDEM	AI	Voltage demodulation pin for data packets based on coil voltage variation
6	QDET	AI	Coil quality factor Detection input
7	CSO	AO	Current sense amplifier output
8	IDEM	AI	Current demodulation pin for data packets based on input current variation
9	VDD33	PO(3.3V)	Regulated 3.3V output used for internal device biasing. Bypass with a 1μF ceramic capacitor to GND
10	VDD18	PO(1.8V)	Regulated 1.8V output used for internal device biasing. Bypass with a 1μF ceramic capacitor to GND
11~16	GPIO0~2,5~7	DIO	General purpose I/O; ADC input pin;
17	VDD	PI(1.8V)	Regulated 1.8V input used for digital core supply. Connect a 1μF capacitor from this pin to GND
18~25	GPIO8~15	DIO	General purpose I/O
26	GPIO18/DM	AIO	General purpose I/O. USB2.0 D+ & D- interface for QC protocol
27	GPIO19/DP	AIO	General purpose I/O. USB2.0 D+ & D- interface for QC protocol
28	CC2	AIO (HV)	Type-c Configuration channel CC1 for PD protocol
29	CC1	AIO(HV)	Type-c Configuration channel CC1 for PD protocol
30	BST1	AI(HV)	Connect a 0.1μF capacitor between BST1 and SW1 to Bootstrap a voltage to provide the bias for high side MOSFET driver.
31	SW1	AO(HV)	Switch node of the half-bridge MOSFET
32	PVIN	PI(HV)	Input voltage for half-bridge MOSFET. Bypass with 22μF ceramic capacitor to GND
33	SW2	AO(HV)	Switch node of the half-bridge MOSFET

34	BST2	AI(HV)	Connect a 0.1μF capacitor between BST2 and SW2 to Bootstrap a voltage to provide the bias for high side MOSFET driver.
35	EPAD	--	The exposed thermal pad should be connected to ground(PGND&GND)

Electrical Characteristic

2.3 Absolute Maximum Ratings

ITEM(V/I)	PIN NAME	MIN	MAX	UNIT
Input Voltage	VIN, PVIN, SW, SW1, SW2	-0.3	24	V
	BST1, BST2	-0.3 -0.3	SW1+6 SW2+6	V V
	CC1, CC2	-0.3	24	V
	TS, CSO, VDEM, IDEM, DP, DM, VDD50, VDD33 GPIO0~ GPIO19	-0.3	6	V
	VDD18	-0.3	2	V
Source Current	EPAD / GND	-0.3	0.3	V
Source /Sink Current	GPIO0~GPIO19	-20	20	mA

2.4 ESD Ratings

TEST MODEL	MIN	MAX	UNIT	NOTE
Human Body Model (HBM)		5	KV	All pins
Charged Device Model (CDM)		500	V	All pins
Machine Model (MM)		200	V	All pins

2.5 Recommended Operating Conditions

RATING	MIN	TYP	MAX	UNIT
Input Operating Range, V_{IN}	4.5	9/12	20	V
Analog voltage Range V_{DD33}	3.0	3.3	3.6	V
Input Voltage Range for GPIO, V_{DD33}	1.8	3.3	3.6	V
Digital voltage range, V_{DD18}	1.62	1.8	1.98	V
Ambient Temperature, T_A	0		85	℃
Junction Temperature, T_J	-20		125	℃

2.6 Electrical Characteristic

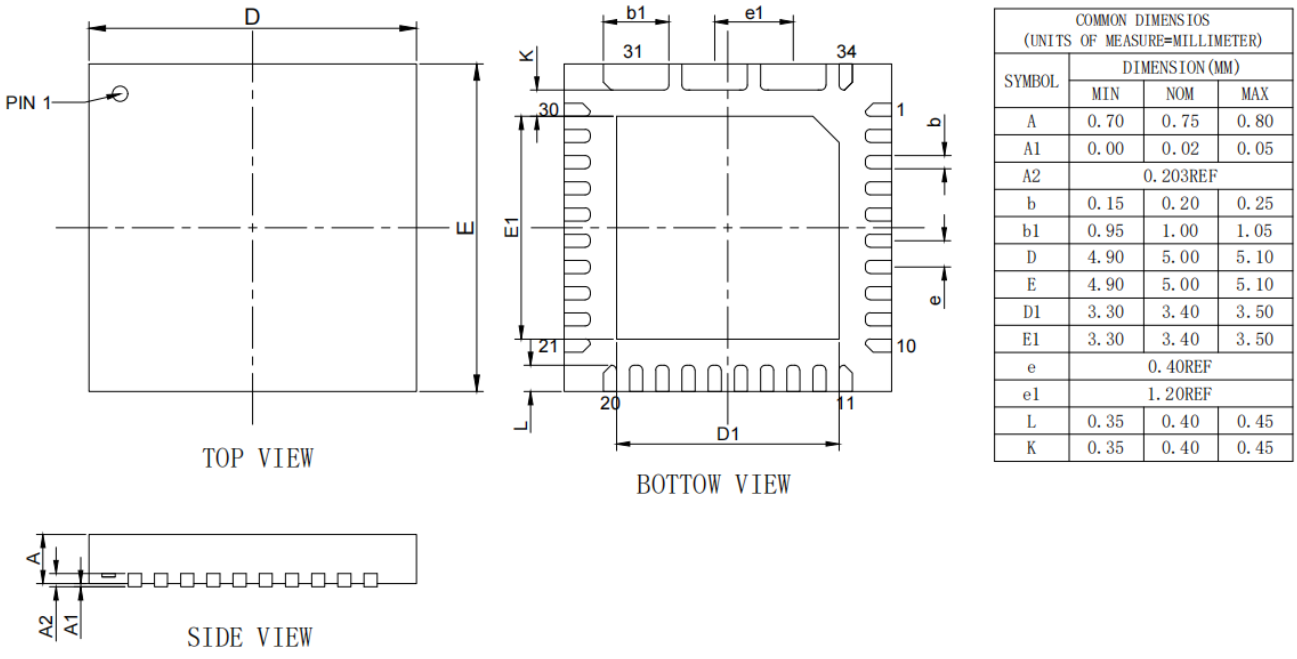
Note: V_{IN} = V_{PVIN} =9V, T_A =25℃, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
System Efficiency (Coupling with RX)					
20W WPT	*V_{IN}=15V, I_{LOAD}=1.56A*		86		%
15W WPT	*V_{IN}=12V, I_{LOAD}=1.3A*		85		%
10W WPT	*V_{IN}=9V, I_{LOAD}=1.1A*		84		%
5W WPT	*V_{IN}=5V, I_{LOAD}=1.0A*		82		%
Input Supply (VIN)					
Input Operating Rang, V_{IN}	*V_{IN} =V_{PVIN}*	4.5	9/ 12	20	V
Operating Mode Current, I_{IN}	*Power Transfer phase, No Load*		30		mA
Standby Mode Current, $I_{STANDBY}$	*Periodic Ping, No Load*		2		mA
Deep sleep Mode Current, I_{DSLEEP}	*No active, No Load*		10		uA
Buck Regulator (VDD50)					
Buck Output Voltage, V_{OUT}	*C_{OUT} = 10μF, L=4.7μH FT Trimming*	4.75	5.0	5.25	V
Buck Output Current, I_{OUT}			50	100	mA
Buck Efficiency, η_{BUCK}	*I_{OUT}=30mA@9V*		85		%
1.8V LDO (VDD18)					
LDO18 Output, V_{DD18}	*FT Trimming*	1.78	1.8	1.82	V
LDO18 Current, I_{DD18}			30		mA
3.3V LDO (VDD33)					
LDO33 Output, V_{DD33}	*FT Trimming*	3.24	3.3	3.36	V
LDO33 Current, I_{DD33}			30		mA
Power MOSFET					
NMOS Turn-On Resistance, R_{DS_ON}	*V_{GS}=4.5V*		25		mΩ
MOSFET driver slew rate	*Programmable, Step=0.25*	0.5	1.0	1.25	V/ns
Dead Time, T_{DEAD}	*Programmable, Step=10ns*	15	45	85	ns
Analog Digital Converter (ADC)					
Resolution, N			11		bit
Sampling Rate, F_S		62.5	250	500	K_{SPS}
Number of Channels, N_{MUX}	*Mux with GPIO0~7*		8		
Full-Scale Range, V_{FS}	*FT Trimming*		1.8		V
HF RC Oscillator (HRC)					
HRC Frequency, F_{HRC}	*Target frequency*		32		MHz
HRC Frequency Accuracy	*FT Trimming*	-1		+1	%
LF RC Oscillator (LRC)					
LRC Frequency, F_{LRC}	*Target frequency*		32		KHz
LRC Frequency Accuracy	*FT Trimming*	-1		+1	%
HF Crystal Oscillator (HXT)					

HXT Frequency, F_{HXT}	*Optional for high accuracy application, Mux GPIO1/2*		16/32		MHz
HXT Frequency Accuracy			20	40	ppm
LF Crystal Oscillator (LXT)					
LXT Frequency, F_{LXT}	*Optional for RTC application Mux GPIO3/4*		32.768		KHz
LXT Frequency Accuracy			50	100	ppm
High Frequency PLL					
PLL Refer Frequency, F_{REF}	*from HRC or HXT*		16		MHz
PLL Frequency Range, F_{PLL}		80	112	160	MHz
Jitter (Phase Noise)			300		ps
Current Sense (ISEN)					
Input Current Range, I_{SEN}	*R_{SENSE}=20mohm*	0		2.5	A
ISEN Gain, I_{SEN_GAIN}	*R_{SENSE}=20mohm*		0.5		V/A
ISEN Gain Error, I_{SEN_GE}	*I_{SENSE} >100mA*	-1%		1%	
Output offset voltage, V_{SENO_OFST}	*After calibration*		*50*		mV
ASK Demodulator					
VDEM input hysteresis voltage, V_{DEM_HYS}	*Programmable, Step=10 mV*	10	64	80	mV
IDEM input hysteresis voltage, I_{DEM_HYS}	*Programmable, Step=10 mV*	10	*64*	80	mV
Q-factor Detector (QDET)					
QDET Detect Voltage, V_{Q_DET}		1.8	3.3	5.0	V
QDET High Threshold, $V_{Q\_TH\_HIGH}$	*Programmable, Step=50 mV*	50	200	400	mV
QDET Low Threshold, $V_{Q\_TH\_LOW}$	*Programmable, Step=50 mV*	25	50	200	mV
Over Current Protection (OCP)					
Over Current Protection,HB- I_{OCP}	*Programmable, Step=1A*	7	10	14	A
Over Current Protection,CS- I_{OCP}	*Programmable, Step=0.2A*	1.6	2.8	3.2	A
VIN Under-Voltage Protection (UVLO)					
Under-Voltage Lockout, V_{IN_UVLO}	*V_{IN} rising Programmable, Step=0.2V*	3.6	4.0	4.2	V
Under-Voltage Hysteresis, V_{IN_UVHYS}	*V_{IN} falling*		0.2/ 0.4		V
VIN Over Voltage Protection (OVP)					
Over Voltage Protection, V_{OVP}	*VIN Rising Programmable, Step=2V*	15	20	25	V
Junction Thermal Protection (OTP)					
Thermal Warning, T_{J_WAR}	*Temp Rising*		120		℃
Thermal Shutdown, T_{J_SD}	*Temp Rising*		140		℃
Hysteresis, T_{J_HYS}	*Temp Falling*		20		℃
DP/DM (QC, AFC)					
DP/DM pull down resistance, R_{DM_DWN}			20		kΩ
DP pin leakage resistance, R_{DP_LKG}			500		kΩ
DP/DM OVP threshold, V_{DPM_OVP}		4.6	4.7	4.8	V

CC1/CC2 (PD)					
CC1/2 pull down resistor, R_{PD_CC}	*$V_{CC1/2}$ = 0V to 2.5V*	*4.59*	*5.1*	*5.61*	kΩ
CC1/2 open impedance, R_{CC_OPEN}	*CC1/2 in disable status*	126			kΩ
CC1/2 OVP threshold, V_{CC_OVP}		*5.8*	*6.1*	*6.4*	V
Digital General-Purpose Input/ Output (GPIO)					
Input Voltage HIGH Level, V_{IH}	*> 0.7*V_{DDIO} (V_{DDIO}= V_{DD33})*	70			%
Input Voltage LOW Level, V_{IL}	*< 0.3*V_{DDIO}*			30	%
Leakage Current, I_{LKG}			1		uA
Output Logic HIGH, V_{OH}	*> 0.9*V_{DDIO}*	90			%
Output Logic LOW, V_{OL}	*< 0.1*V_{DDIO}*			10	%
Source Current, I_{SRC}	*V_{GS}=3.3V, R_{ON}=100Ω*		4/12		mA
Sink Current, I_{Sink}	*V_{GS}=3.3V, R_{ON}=80Ω*		4/12		mA

3. Package information



COMMON DIMENSIOS (UNITS OF MEASURE=MILLIMETER)			
SYMBOL	DIMENSION (MM)		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.203REF		
b	0.15	0.20	0.25
b1	0.95	1.00	1.05
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D1	3.30	3.40	3.50
E1	3.30	3.40	3.50
e	0.40REF		
e1	1.20REF		
L	0.35	0.40	0.45
K	0.35	0.40	0.45

Figure 3 OPS1033 Package information