# 24-Bit, 192kHz立体声D/A转换器

## ■ FEATURES

- 支持多种音频数字输入格式，最大支持24-bit字节
- 可自动检测采样频率，最高192kHz
- 105dB动态范围
- -90dB THD+N
- 集成多比特位的Δ-Σ调制器
- 支持3.3V/5V单电源供电
- 具有强抗时钟抖动能力
- 内部集成输出滤波
- 集成数字去重，外部无需SCLK
- 输出pop声抑制
- TSSOP14封装

## ■ APPLICATIONS

- 音响 · DVD · 电视机
- 机顶盒 · 数码相框 · 家庭影院

## ■ DESCRIPTION

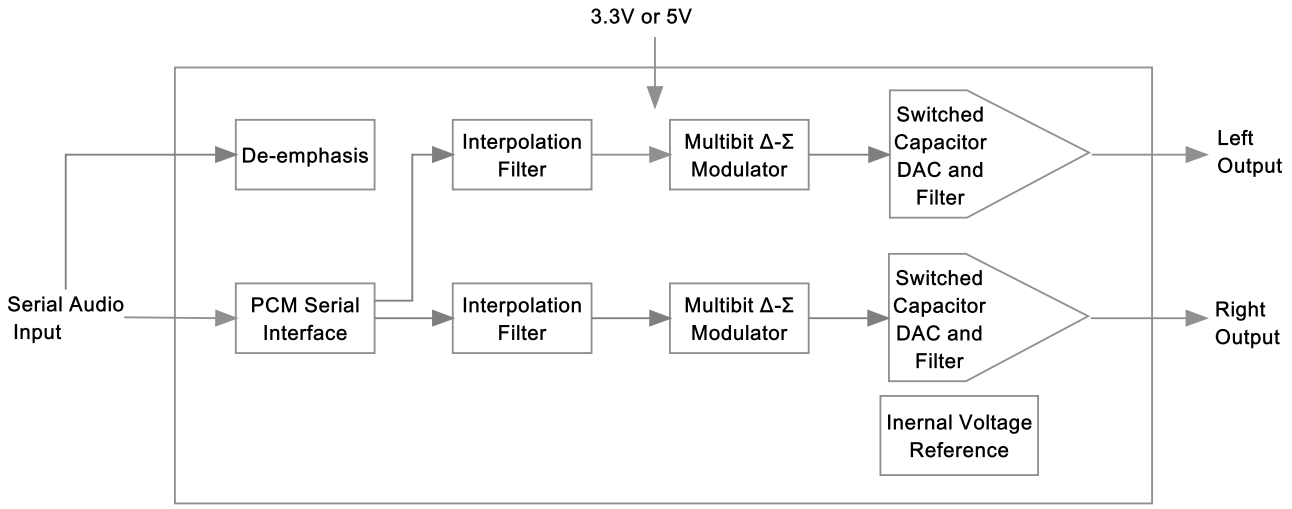
HT4344系列产品是一款低成本的立体声DA转换器，内部集成了内插滤波器、DA转换器和输出模拟滤波等电路。其可支持多种音频数字输入格式，最大支持24-bit字节。

该系列产品基于一个多比特位的Δ-Σ调制器，将数字信号转化成两个声道的模拟信号并经过模拟滤波器滤波。该Δ-Σ调制器对时钟抖动的敏感度很低，且在带宽范围外具有极低的噪声。其还可使用采样率和主时钟比作为自采样率（2kHz – 200kHz），从而实现自动检测采样频率的功能。

该系列产品还集成了数字去重，3.3V/5V单电源供电，无需外部SCLK，简化了外围电路，适用于DVD、数字电视、家庭影院、机顶盒等。

该系列产品为TSSOP14封装。

## ■ BLOCK DIAGRAM



# 24-Bit, 192kHz Stereo D/A Converter

## ■ FEATURES

- Multiple audio data interface formats, up to 24-bit
- Automatically Detects Sample Rates up to 192kHz
- 105dB Dynamic Range
- -90dB THD+N
- Multi-bit Delta-Sigma Modulator
- 3.3V or 5V Single Power Supply
- Low Clock-Jitter Sensitivity
- Filtered Line-Level Outputs
- On-chip Digital De-emphasis
- Output pop-noise Minimization
- Small 14-pin TSSOP Package

## ■ APPLICATIONS

- Speakers
- TV sets
- DVD Player
- Set top box
- Digital Photo Frame
- DVD recorder
- Home theater
- Automotive audio system

## ■ DESCRIPTION

The HT4344 family is a low-cost stereo digital to analog converter, including interpolation, multibit D/A conversion and output analog filtering in a 14-pin package.

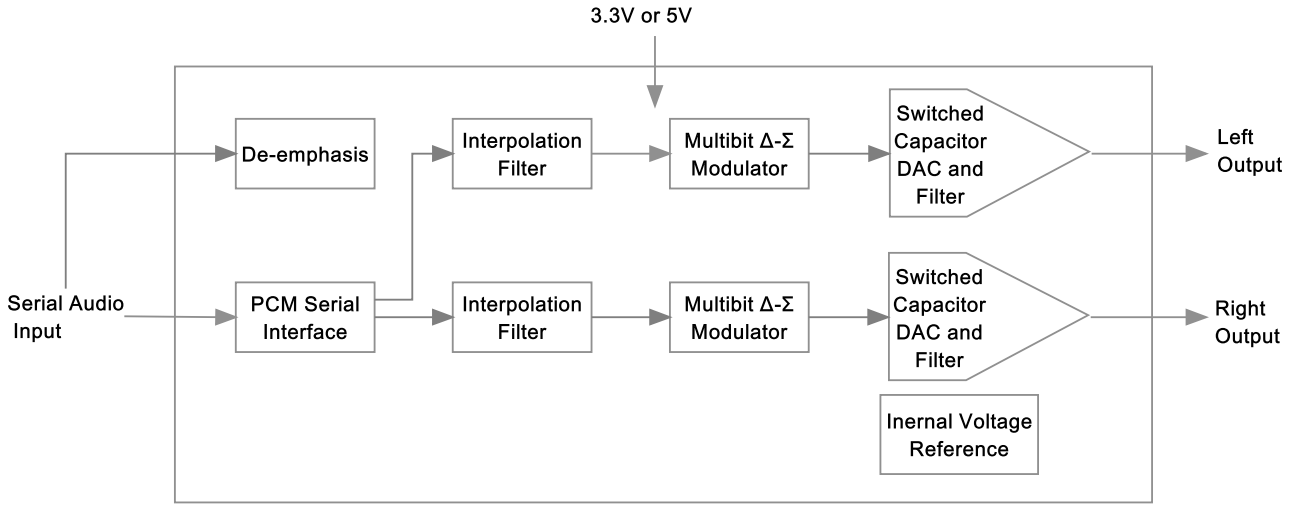
The device family can accept multiple audio formats up to 24-bit word length.

The device family is based on an advanced multi-bit Δ-Σ modulator to convert data into two channel analog outputs with a linear analog low-pass filter. The multi-bit Δ-Σ modulator makes the device with very low sensitivity to clock jitter and very low out-of-band noise. It also includes auto speed mode detection using both sample rate and master clock ratio as a method of auto-selecting sampling rates between 2 kHz and 200 kHz.

The device family contains on-chip digital deemphasis, operates from a single +3.3V or +5V power supply, and requires minimal support circuitry. These features are ideal for DVD players & recorders, digital televisions, home theater and set top box products, and automotive audio systems.

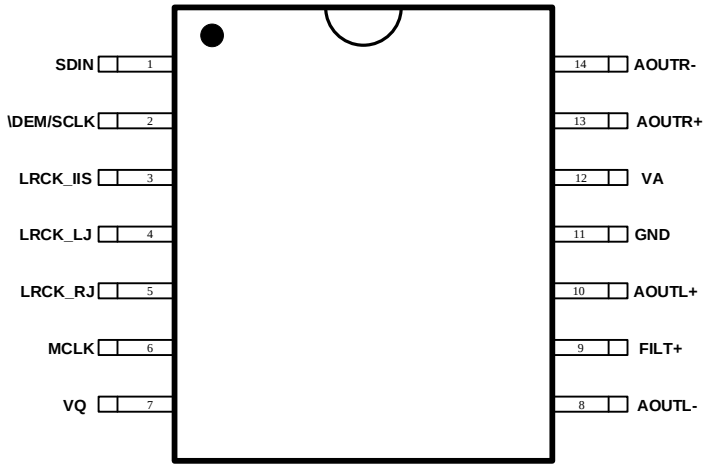
The device family is available in a 14-pin TSSOP14 package.

## ■ BLOCK DIAGRAM



# Contents

## ■ TERMINAL CONFIGURATION




## ■ TERMINAL FUNCTION

| Terminal No. | NAME | I/O[1] | Description |
|---|---|---|---|
| 1 | SDIN | I | Serial audio data input. |
| 2 | $\overline{\text{DEM}}$/SCLK | I | De-emphasis / external serial clock input |
| 3 | LRCK_IIS | I | Left right clock for $I^2S$ serial audio data |
| 4 | LRCK_LJ | I | Left right clock for Left Justified serial audio data |
| 5 | LRCK_RJ | I | Left right clock for Right Justified serial audio data |
| 6 | MCLK | I | Master clock |
| 7 | VQ | O | Filter connection for internal quiescent voltage |
| 8 | AOUTL- | O | Left channel analog output (differential -) |
| 9 | FILT+ | O | Positive reference voltage for the internal sampling |
| 10 | AOUTL+ | O | Left channel analog output (differential +) |
| 11 | GND | G | Ground |
| 12 | VA | P | Analog power supply |
| 13 | AOUTR+ | O | Right channel analog output (differential +) |
| 14 | AOUTR- | O | Right channel analog output (differential -) |

## ■ ORDERING INFORMATION

| Part Number | Package Type | Marking | Operating Temperature Range | Container |
|---|---|---|---|---|
| HT4344MTR | TSSOP14 | HT4344<br>UVWXYZ[2] | -40℃～85℃ | Tape and Reel |

[1] I: input O: output G: GNDP: Power

[2] UVWXYZ is production track code.

## ■ ELECTRICAL CHARACTERISTICS[3]

### ● Absolute Maximum Ratings[4]

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage range | VA | -0.3 | 5.5 | V |
| Digital input voltage range | $V_{IN}$ | -0.3 | VA+0.3 | V |
| Input current, any pin except supplies | $I_{IN}$ | - | ±10 | mA |
| Operating temperature range | $T_A$ | -40 | 85 | ℃ |
| Operating junction temperature range | $T_J$ | -40 | 150 | ℃ |
| Storage temperature range | $T_{STG}$ | -50 | 150 | ℃ |

### ● Recommended Operating Conditions

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Supply voltage range | VA | | 3.0<br>4.75 | 3.3<br>5.0 | 3.6<br>5.25 | V |
| Operating temperature | $T_a$ | | -40 | 25 | 85 | ℃ |

### ● Dynamic Performance

Condition: Fs = 48/96/192kHz, input 0dB 1kHz, Load $R_L$ = 3kohm, $C_L$ = 10pF, unless otherwise specified.

| PARAMETER | SYMBOL | CONDITION | | VA = 3.3V | | | VA = 5V | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Dynamic Range | DR | 18 to 24-bit, A weighted | | | 103 | | | 105 | | dB |
| | | 16-Bit, A-weighted | | | 96 | | | 96 | | |
| Total Harmonic Distortion + Noise | THD+N | 18 to 24-bit | 0dB input | | -90 | | | -90 | | dB |
| | | | -20 dB input | | -80 | | | -82 | | dB |
| | | | -60 dB input | | -40 | | | -42 | | dB |
| | | 16-bit | 0dB input | | -90 | | | -90 | | dB |
| | | | -20 dB input | | -73 | | | -73 | | dB |
| | | | -60 dB input | | -33 | | | -33 | | dB |

### ● Analog Performance

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Cross Talk | CT | 1kHz | | 103 | | dB |
| Inter-channel Gain Mismatch | / | | | 0.1 | | dB |
| Gain Drift | / | | | 100 | | ppm/℃ |
| Full Scale Output Voltage | / | | 1.2×VA | 1.3×VA | 1.4×VA | Vpp |
| Quiescent Voltage | $V_Q$ | | | 0.5×VA | | VDC |
| Max DC Current draw from an AOUT pin | $I_{OUTmax}$ | | | 10 | | uA |
| Max Current draw from VQ | $I_{Qmax}$ | | | 100 | | uA |
| Max AC-Load Resistance | $R_L$ | | | 3 | | KΩ |
| Max Load Capacitance | $C_L$ | | | 100 | | pF |
| Output Impedance | $Z_{OUT}$ | | | 100 | | Ω |

[3] Depending on parts and PCB layout, characteristics may be changed.

[4] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability

## ● Combined Interpolation & on-chip analog filter response

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| ***Single-speed mode*** | | | | | | |
| Passband | / | to -0.1dB corner | 0 | | 0.35 | Fs |
| | | to -3dB corner | 0 | | 0.4992 | Fs |
| Frequency response | / | 10Hz to 20kHz | -0.175 | | +0.01 | dB |
| Stop band | / | | 0.5465 | | | Fs |
| Stop band attenuation | / | Measurement Bandwidth is 0.5465 Fs to 3 Fs | 50 | | | dB |
| Group Delay | tgd | | | 10/Fs | | s |
| De-emphasis Error (De-emphasis is only available in Single-speed mode) | / | Fs = 32kHz | | | +1.5/+0 | dB |
| | | Fs = 44.1kHz | | | +0.05/-0.25 | |
| | | Fs = 48kHz | | | -0.2/-0.4 | |
| ***Double-speed mode*** | | | | | | |
| Passband | / | to -0.1dB corner | 0 | | 0.22 | Fs |
| | | to -3dB corner | 0 | | 0.501 | Fs |
| Frequency response | / | 10Hz to 20kHz | -0.15 | | +0.15 | dB |
| Stop band | / | | 0.5770 | | | Fs |
| Stop band attenuation | / | Measurement Bandwidth is 0.5465 Fs to 3 Fs | 55 | | | dB |
| Group Delay | tgd | | | 5/Fs | | s |
| ***Quad-speed mode*** | | | | | | |
| Passband | / | to -0.1dB corner | 0 | | 0.11 | Fs |
| | | to -3dB corner | 0 | | 0.469 | Fs |
| Frequency response | / | 10Hz to 20kHz | -0.12 | | +0 | dB |
| Stop band | / | | 0.4 | | | Fs |
| Stop band attenuation | / | Measurement Bandwidth is 0.5465 Fs to 3 Fs | 51 | | | dB |
| Group Delay | tgd | | | 2.5/Fs | | s |

## ● Digital Input Characteristics

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| High-level Input Voltage | $V_{IH}$ | | 60% | | | VA |
| Low-level Input Voltage | $V_{IL}$ | | | | 30% | VA |
| Input Leakage Current | $I_{in}$ | except LRCK | | | ±10 | uA |
| | | LRCK | | | ±20 | uA |
| Input Capacitance | / | | | 8 | | pF |

## ● Power and Thermal Characteristics

Condition: VA = 3.3V

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Power supply current[5] | $I_A$ | Normal operation | | 16 | | mA |
| | | Power-down state[6] | | 100 | | uA |
| Power dissipation | $P_D$ | Normal operation | | 53 | | mW |
| | | Power-down state[6] | | 0.33 | | mW |
| Package Thermal Resistance | $\theta_{JA}$ | | | 95 | | ℃/W |
| Power supply rejection ratio | PSRR | 1kHz | | 50 | | dB |
| | | 60Hz | | 40 | | dB |

[5] Current consumption will increase with increasing FS and MCLK.
[6] Power-down state is defined when all clock and data lines are held static.

Condition: VA = 5V

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Power supply current[7] | $I_A$ | Normal operation | | 20 | | mA |
| | | Power-down state[8] | | 180 | | uA |
| Power dissipation | $P_D$ | Normal operation | | 100 | | mW |
| | | Power-down state | | 0.9 | | mW |
| Package Thermal Resistance | $\theta_{JA}$ | | | 95 | | ℃/W |
| Power supply rejection ratio | PSRR | 1kHz | | 44 | | dB |
| | | 60Hz | | 40 | | dB |

## ● Serial Audio Interface Switching Characteristics

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| MCLK Frequency | $f_{MCLK}$ | | 0.512 | | 50 | MHz |
| MCLK Duty Cycle | $D_{MCLK}$ | | 45 | | 55 | % |
| Input Sample Rate[9] | $F_S$ | All MCLK/LRCK ratios combined | 2 | | 200 | kHz |
| | | 256x, 384x, 1024x | 2 | | 50 | kHz |
| | | 256x, 384x | 84 | | 134 | kHz |
| | | 512x, 768x | 42 | | 67 | kHz |
| | | 1152x | 30 | | 34 | kHz |
| | | 128x, 192x | 50 | | 100 | kHz |
| | | 64x, 96x | 100 | | 200 | kHz |
| | | 128x, 192x | 168 | | 200 | kHz |
| ***External SCLK Mode*** | | | | | | |
| LRCK Duty Cycle | $D_{LRCK}$ | | 45 | 50 | 55 | % |
| SCLK Pulse Width Low | $T_{sclkl}$ | | 20 | | | ns |
| SCLK Pulse Width High | $T_{sclkh}$ | | 20 | | | ns |
| SCLK Duty Cycle | $D_{SCLK}$ | | 45 | 50 | 55 | % |
| SCLK rising to LRCK edge delay | $t_{slrd}$ | | 20 | | | ns |
| SCLK rising to LRCK edge setup time | $t_{slrs}$ | | 20 | | | ns |
| SDIN valid to SCLK rising setup time | $t_{sdlrs}$ | | 20 | | | ns |
| SCLK rising to SDIN hold time | $t_{sdh}$ | | 20 | | | ns |
| ***Internal SCLK Mode*** | | | | | | |
| LRCK Duty Cycle[10] | $D_{LRCK}$ | | | 50 | | % |
| SCLK Period | $t_{sclkw}$ | | $\frac{10^9}{SCLK}$ | | | ns |
| SCLK rising to LRCK edge | $t_{sclkr}$ | | | $t_{sclkw}/2$ | | ns |
| SDIN valid to SCLK rising setup time | $t_{sdlrs}$ | | $\frac{10^9}{512F_s}+10$ | | | ns |
| SCLK rising to SDIN hold time | $t_{sdh}$ | MCLK / LRCK =1152, 1024, 512, 256, 128, or 64 | $\frac{10^9}{512F_s}+15$ | | | ns |

[7] Current consumption will increase with increasing FS and MCLK.
[8] Power-down state is defined when all clock and data lines are held static.
[9] Not all sample rates are supported for all clock ratios. See Table 2 for detail.
[10] In internal SCLK mode, the duty cycle must be 50% ± 1/2 MCLK period.

| | | | | | | |
|---|---|---|---|---|---|---|
| SCLK rising to SDIN hold time | $t_{sdh}$ | MCLK / LRCK = 768, 384, 192, or 96 | $\frac{10^9}{384F_s} + 15$ | | | ns |

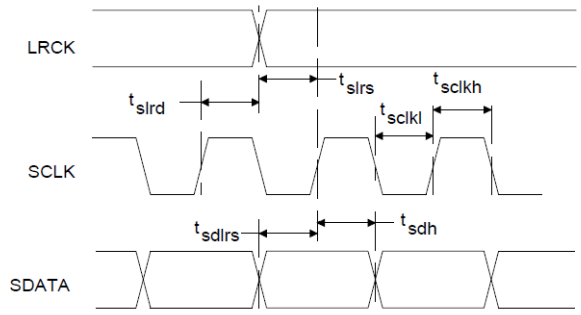



Figure 1 External Serial Mode Input Timing

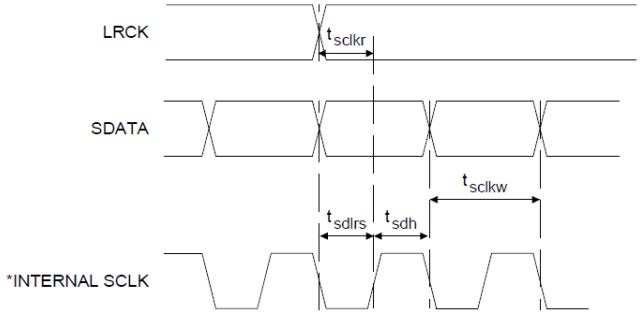



Figure 2 External Serial Mode Input Timing

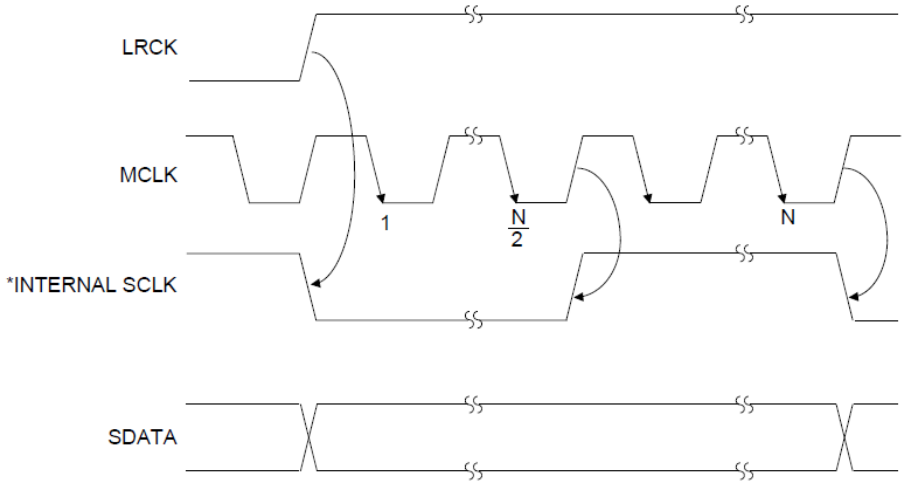


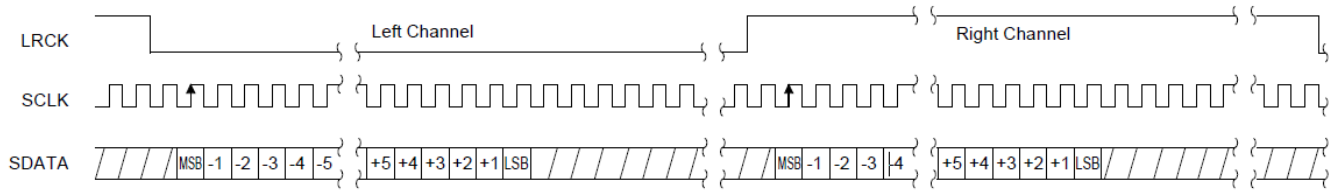

Figure 3 Internal Serial Clock Generation (N equals MCLK divided by SCLK)

## ■ APPLICATION INFORMATION

The HT4344 family accepts data at standard audio sample rates including 48, 44.1 and 32 kHz (also 24k, 16k, 12k and 8k if high quality THD+N is not required) in Single-Speed Mode (SSM), 96, 88.2 and 64 kHz in Double-Speed Mode (DSM), and 192, 176.4 and 128 kHz in Quad-Speed Mode (QSM). Audio data is input via the serial data input pin (SDIN). The Left/Right Clock (LRCK) determines which channel is currently being input on SDIN, and the optional Serial Clock (SCLK) clocks audio data into the input data buffer. The HT4344 differ in serial data formats as shown in the following Table 1.

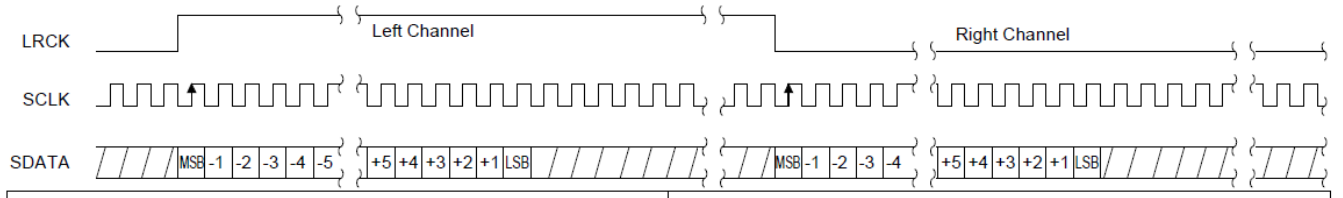
Table 1 HT4344 can accept multiple audio data interface formats

| | |
|---|---|
| I²S | Accept 16 to 24-bit I²S serial audio data |
| Left Justified | Accept 16 to 24-bit Left Justified serial audio data |
| Right Justified | Accept 16-bit Right Justified serial audio data |



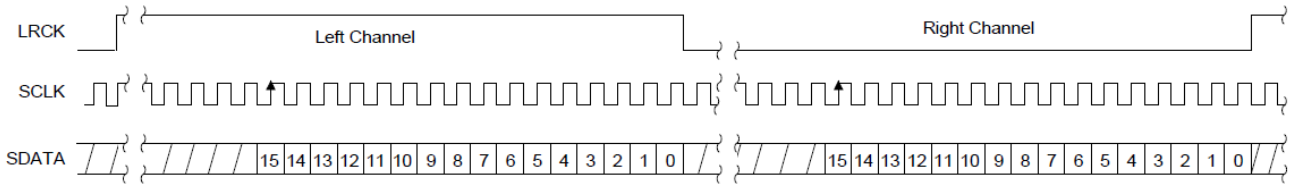

| Internal SCLK Mode | External SCLK Mode |
|---|---|
| I²S, 16-Bit data and INT SCLK = 32 Fs if<br>MCLK/LRCK = 1024, 512, 256, 128, or 64<br>I²S, Up to 24-Bit data and INT SCLK = 48 Fs if<br>MCLK/LRCK = 768, 384, 192, or 96<br>I²S, Up to 24-Bit data and INT SCLK = 72 Fs if<br>MCLK/LRCK = 1152 | I²S, up to 24-Bit Data<br>Data Valid on Rising Edge of SCLK |

Figure 4 I²S Data Format




| Internal SCLK Mode | External SCLK Mode |
|---|---|
| Left-Justified, up to 24-Bit Data<br>INT SCLK = 64 Fs if<br>MCLK/LRCK = 1024, 512, 256, 128, or 64<br>INT SCLK = 48 Fs if<br>MCLK/LRCK = 768, 384, 192, or 96<br>INT SCLK = 72 Fs if<br>MCLK/LRCK = 1152 | Left-Justified, up to 24-Bit Data<br>Data Valid on Rising Edge of SCLK |

Figure 5 Left Justified Data Format




| Internal SCLK Mode | External SCLK Mode |
|---|---|
| Right Justified, 16-Bit Data<br>INT SCLK = 32 Fs if<br>MCLK/LRCK = 1024, 512, 256, 128, or 64<br>INT SCLK = 48 Fs if<br>MCLK/LRCK = 768, 384, 192, or 96<br>INT SCLK = 72 Fs if<br>MCLK/LRCK = 1152 | Right Justified, 16-Bit Data<br>Data Valid on Rising Edge of SCLK<br>SCLK Must Have at Least 32 Cycles per LRCK Period |

Figure 6 Right Justified 16-bit Data Format

### *1. Master Clock*

MCLK/LRCK must be an integer ratio, as shown in Table 2.

Table 2 Common Clock Frequencies

| LRCK (kHz) | MCLK(MHz) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 64× | 96× | 128× | 192× | 256× | 384× | 512× | 768× | 1024× | 1152× |
| 8 | | | | | 2.0480 | 3.0720 | 4.0960 | 6.1440 | - | - |
| 12 | | | | | 3.0720 | 4.6080 | 6.1440 | 9.2160 | - | - |
| 16 | | | | | 4.0960 | 6.1440 | 8.1920 | 12.2880 | 16.3840 | - |
| 24 | | | | | 6.1440 | 9.2160 | 12.2880 | 18.4320 | 24.5760 | - |
| 32 | - | - | - | - | 8.1920 | 12.2880 | - | - | 32.7680 | 36.8640 |
| 44.1 | - | - | - | - | 11.2896 | 16.9344 | 22.5792 | 33.8680 | 45.1580 | - |
| 48 | - | - | - | - | 12.2880 | 18.4320 | 24.5760 | 36.8640 | 49.1520 | - |
| 64 | - | - | 8.1920 | 12.2880 | - | - | 32.7680 | 49.1520 | - | - |
| 88.2 | - | - | 11.2896 | 16.9344 | 22.5792 | 33.8680 | - | - | - | - |
| 96 | - | - | 12.2880 | 18.4320 | 24.5760 | 36.8640 | - | - | - | - |
| 128 | 8.1920 | 12.2880 | - | - | 32.7680 | 49.1520 | - | - | - | - |
| 176.4 | 11.2896 | 16.9344 | 22.5792 | 33.8680 | - | - | - | - | - | - |
| 192 | - | 18.4320 | 24.5760 | 36.8640 | - | - | - | - | - | - |
| Mode | QSM | | | | DSM | | SSM | | | |

The LRCK frequency is equal to Fs, the frequency at which words for each channel are input to the device. The MCLK-to-LRCK frequency ratio and speed mode is detected automatically during the initialization sequence by counting the number of MCLK transitions during a single LRCK period and by detecting the

absolute speed of MCLK. Internal dividers are set to generate the proper clocks. Table 2 illustrates several standard audio sample rates and the required MCLK and LRCK frequencies. Please note there is no required phase relationship, but MCLK, LRCK and SCLK must be synchronous.

### *2. Serial Clock*

The serial clock controls the shifting of data into the input data buffers. The HT4344 family supports both external and internal serial clock generation modes. Refer to Figure 4 - Figure 6 for data formats.

### *2.1. External Serial Clock Mode*

The HT4344 family will enter the External Serial Clock Mode when 16 low to high transitions are detected on the DEM/SCLK pin during any phase of the LRCK period. When this mode is enabled, the Internal Serial Clock Mode and de-emphasis filter cannot be accessed. The HT4344 family will switch to Internal Serial Clock Mode if no low to high transitions are detected on the DEM/SCLK pin for 2 consecutive frames of LRCK.

### *2.2. Internal Serial Clock Mode*

In the Internal Serial Clock Mode, the serial clock is internally derived and synchronous with MCLK and LRCK. The SCLK/LRCK frequency ratio is either 32, 48, 64, or 72 depending upon data format. Operation in this mode is identical to operation with an external serial clock synchronized with LRCK. This mode allows access to the digital deemphasis function. Refer to Figure 4 - Figure 6 for details.

### *3. De-Emphasis*

The HT4344 family includes on-chip digital de-emphasis. Figure 7 shows the de-emphasis curve for Fs equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs.

The de-emphasis filter is active (inactive) if the DEM/SCLK pin is low (high) for 5 consecutive falling edges of LRCK. This function is available only in the internal serial clock mode

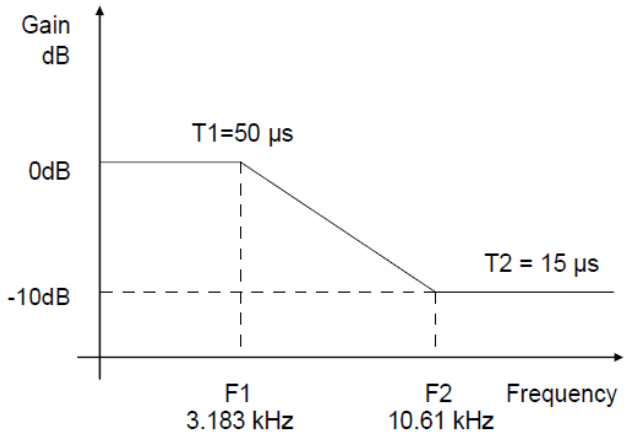



Figure 7 De-emphasis Curve (Fs = 44.1kHz)

### *4. Initialization and Power-down*

The Initialization and Power-down sequence flow chart is shown in Figure 8. The HT4344 family enters the Power-Down State upon initial power-up. The interpolation filters and delta-sigma modulators are reset, and the internal voltage reference, multi-bit digital-to-analog converters and switched-capacitor low-pass filters are powered down. The device will remain in the Power-down mode until MCLK and LRCK are present. Once MCLK and LRCK are detected, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio. Power is then applied to the internal voltage reference. Finally, power is applied to the D/A converters and switched-capacitor filters, and the analog outputs will ramp to the quiescent voltage, VQ.

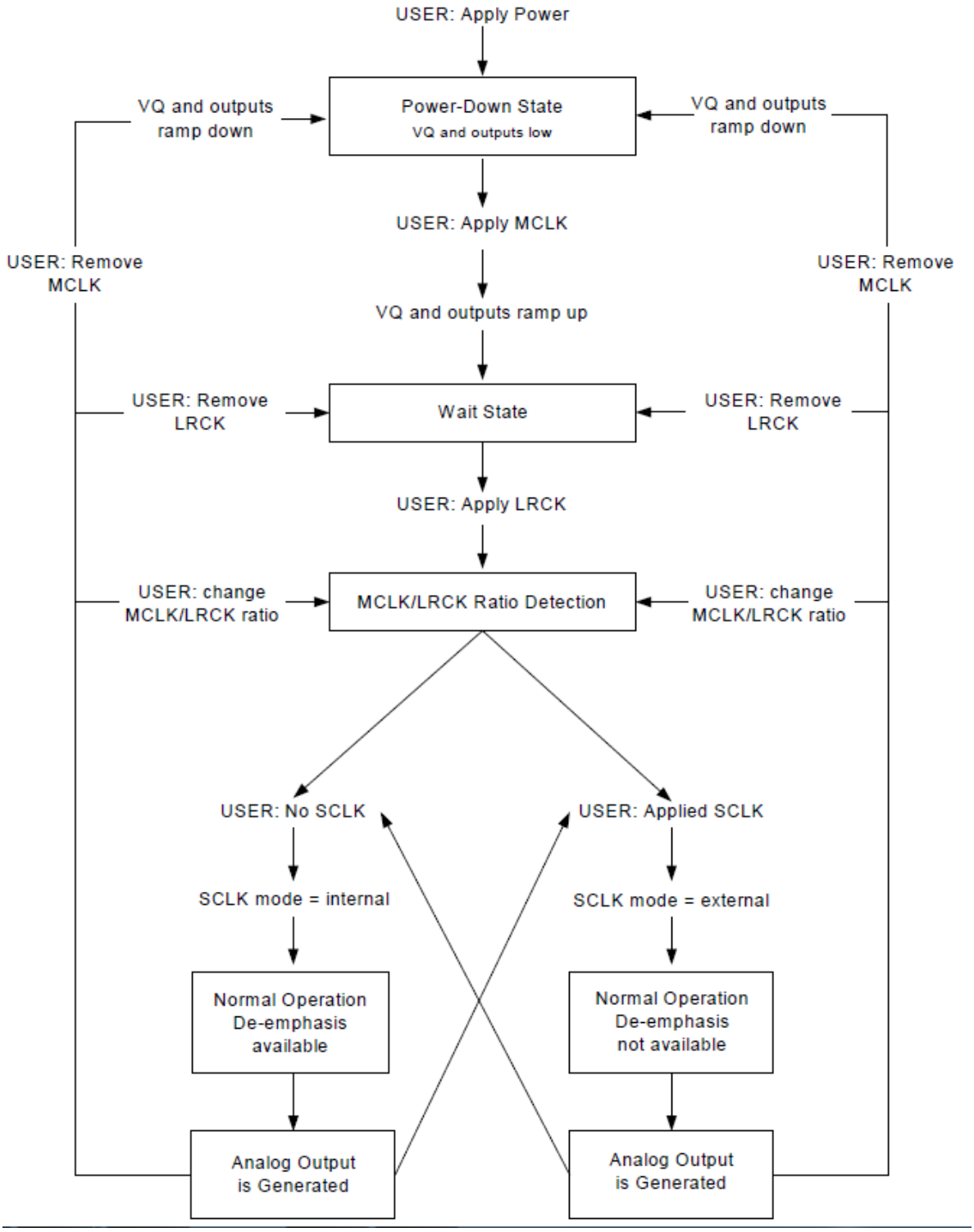



Figure 8 Initialization and Power-down Sequence

### *5. Output Pop Noise Control*

The HT4344 family can minimize the output pop noise during powerup and power-down, that is commonly produced by single-ended single-supply converters when it is implemented with external DC-blocking capacitors connected in series with the audio outputs. To make best use of this feature, it is necessary to understand its operation.

### *5.1. Powerup*

When the device is initially powered-up, the audio outputs, AOUTL and AOUTR, are clamped to VQ which

is initially low. After MCLK is applied, the outputs begin to ramp with VQ towards the nominal quiescent voltage. This ramp takes approximately 680 ms with a 3.3 µF cap connected to VQ (860 ms with a 10 µF connected to VQ) to complete. The gradual voltage ramping allows time for the external DC-blocking capacitors to charge to VQ, effectively blocking the quiescent DC voltage. Once valid LRCK and SDIN are supplied (and SCLK if used) approximately 2000 sample periods later audio output begins.

### *5.2. Power-down*

To prevent pop noise at power-down, the DC-blocking capacitors must fully discharge before turning off the power. To accomplish this, MCLK should be stopped for a period of about 680 ms for a 3.3 µF capacitor connected to VQ (860 ms for a 10 µF cap connected to VQ) before removing power. During this time voltage on VQ and the audio outputs discharge gradually to GND. If power is removed before this time period has passed, pop noise will occur when the VA supply drops below that of VQ. There is no minimum time for a power cycle; power may be re-applied at any time.

When changing clock ratio or sample rate, it is recommended that zero data (or near zero data) be present on SDIN for at least 10 LRCK samples before the change is made. During the clocking change, the DAC outputs will always be in a zero data state. If no zero audio is present at the time of switching, a slight click or pop may be heard as the DAC output automatically goes to its zero data state.

### *6. Grounding and Power Supply Decoupling*

As with any high-resolution converter, the HT4344 family requires careful attention to power supply and grounding arrangements to optimize performance. Figure 9 shows the recommended power arrangement with VA connected to a clean +3.3 V or +5.5V supply. For best performance, decoupling and filter capacitors should be located as close to the device package as possible with the smallest capacitors closest.

### *7. Analog Output and Filtering*

The analog filter present in the HT4344 family is a switched-capacitor filter followed by a continuous time low pass filter. The recommended external analog circuitry is shown in the Figure 9.

### *8. Typical Application*

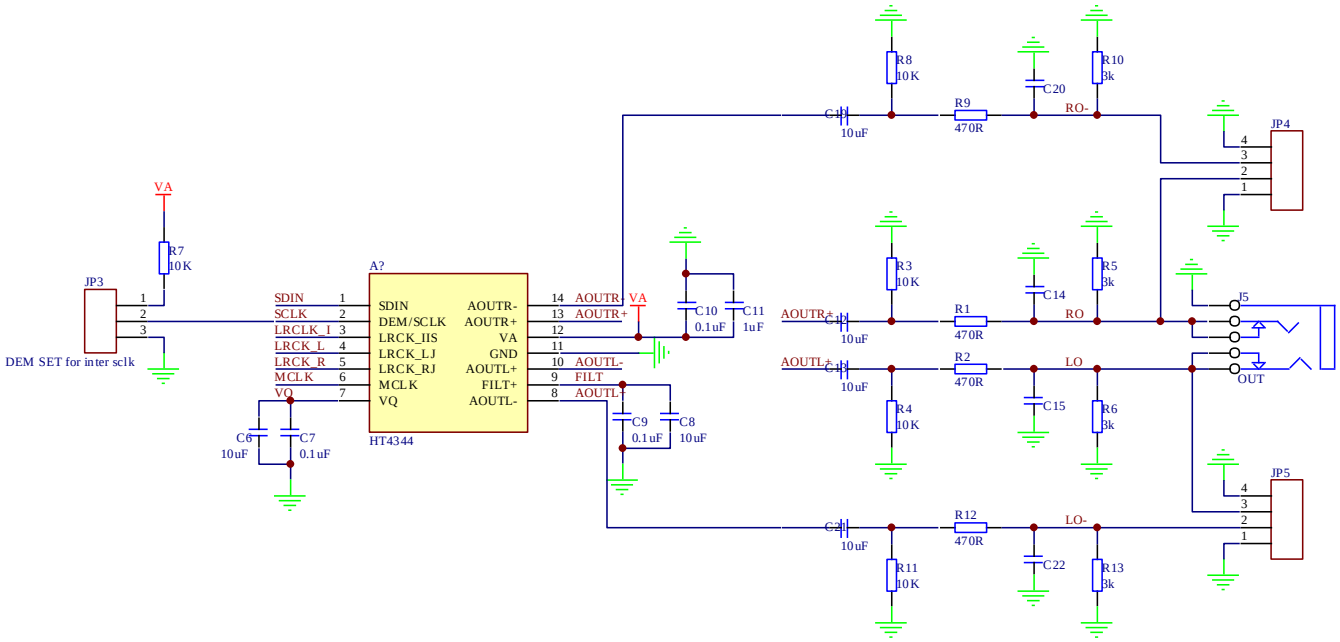
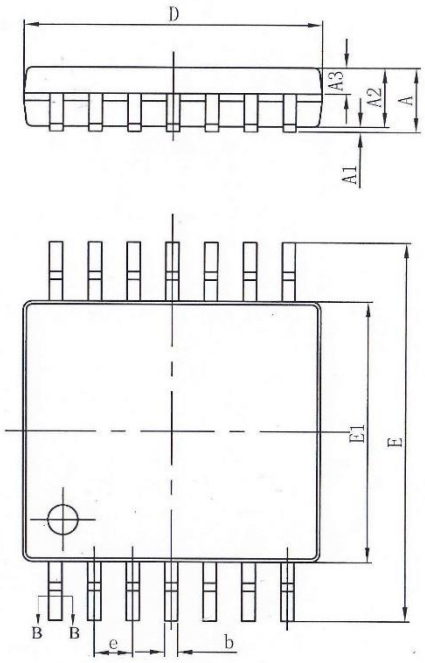
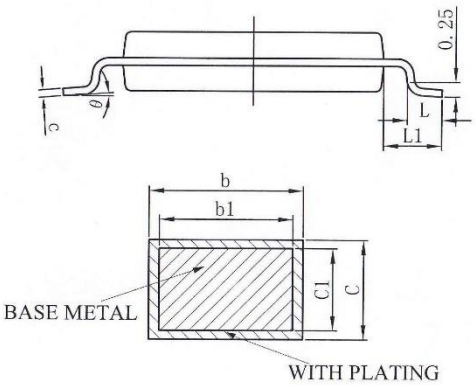



Figure 9 Typical Application

## ■ PACKAGE OUTLINE

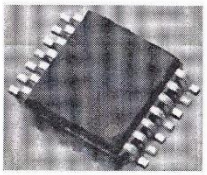






SECTION B-B



| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.90 | 1.00 | 1.05 |
| A3 | 0.39 | 0.44 | 0.49 |
| b | 0.20 | — | 0.28 |
| b1 | 0.19 | 0.22 | 0.25 |
| c | 0.13 | — | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 4.90 | 5.00 | 5.10 |
| E1 | 4.30 | 4.40 | 4.50 |
| E | 6.20 | 6.40 | 6.60 |
| e | 0.65BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00BSC | | |
| θ | 0 | — | 8° |

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